A 4-bit Ultra-Wideband Beamformer with 4ps True Time Delay Resolution

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***Abstract*— This paper documents an ultra-wideband (UWB) fully integrated beamformer which features controllable true time delay and power gain. The UWB beamformer accomplishes 4-bit delay variation with 4ps resolution, 5dB gain variation in 1dB steps, and a -3dB gain bandwidth of 11.2GHz. Overall operation is achieved by the integration of a three-bit tapped delay trombone-type structure with 4ps variable delay resolution, a one-bit 32ps fixed delay coplanar-type structure, and a variable gain distributed amplifier. The prototype chip fabricated in a 0.18μm BiCMOS SiGe process occupies 1.6mm^2 of silicon area and consumes 125mW from a 2.5V supply at the maximum gain setting of 14.2dB.**

***Index Terms*— Microwave antenna arrays, beam steering, delay circuits, BiCMOS integrated circuits.**

I. Introduction

Beamforming is a technique which utilizes variable time delay and gain to accomplish sidelobe suppression and selective nulling in multi-antenna systems. In narrowband phased array systems, the variable time delay is often approximated with a phase-shifter to ease the implementation [1]. While phase shifting is sufficient for many narrowband applications, it fails to mimic the true time delay needed in ultra-wideband (UWB) multi-antenna systems. UWB phased arrays offer numerous applications, namely, high-resolution imaging, accurate ranging, and high data-rate communication for wireless local area networks.

In a phased-array system, the electromagnetic wave reaches each antenna element at a time that depends on the incidence angle. The delay associated with any electromagnetic signal is the traveled distance divided by wave velocity. Thus, variable time delay on a standard semiconductor process can be achieved through either actively manipulating the velocity of the signal and/or varying the path length . The work presented in this paper achieves true time delay operation through the latter and is presented as follows. Section II details the UWB beamformer system design methodology and its associated circuitry. Measured performance of the fabricated beamformer is reported in section III followed by concluding remarks in section IV.

II. UWB Beamformer Design

A. System Architecture

A system level representation of the beamformer is featured in Fig. 1. There are four main subsystems that contribute to the overall functionality. A "trombone" delay structure, which is typically realized through mechanical means, was designed as a tapped delay topology (Fig. 2) in order to yield a total of 32ps delay variation in τ=4ps increments (3-bit control). In an UWB phased-array system, the overall requirement is not only to have a small time delay resolution, but also to achieve a large total delay. For a fixed delay resolution, the tapped delay version of the trombone line suffers from loss and significant delay variation as the total delay is increased. Thus, to increase the total delay, a switchable coplanar transmission line structure, referred to as the "eight-tau" (8-τ) section, is added to provide 32ps of delay (i.e., coarse tuning). The overall beamformer variable delay is 64ps with 4ps resolution corresponding to 4-bits. To accomplish sidelobe suppression in an UWB phased array, a variable gain should also be included to complete the beamformer functionality. In this implementation, an UWB variable gain distributed amplifier (VGDA) is used to control the power gain within 5dB in 1dB steps. In addition, the chip features an on-chip programable digital control unit (DCU) and temperature and supply independent biasing. All delay elements in the tapped trombone line and the VGDA were constructed with lumped *LC* elements rather than a microstrip or coplanar approach. The operating frequencies, desired delay resolution, and real estate overhead did not warrant implementing the delay with true transmission lines. The choice of *L* and *C* values is uniquely determined by the

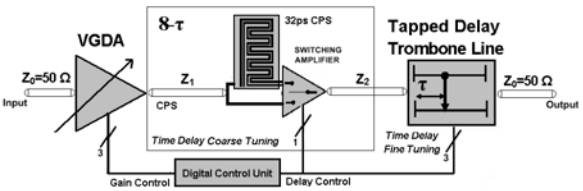

Fig. 1. Beamformer system block diagram.

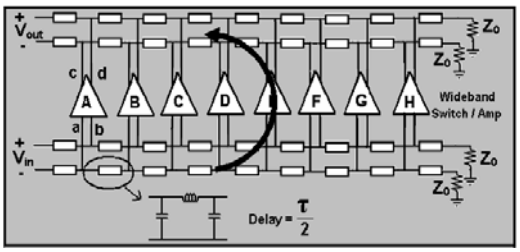

Fig. 2. The 3-bit tapped delay trombone line.

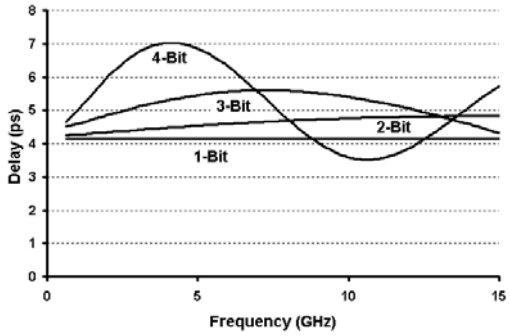

Fig. 3. Simulated delay flatness of trombone lines as the bit order is increased.

characteristic impedance given by ($Z_0 = \sqrt{L/C}$), the desired delay resolution ($\tau = 2\sqrt{LC}$) for the trombone line, and the bandwidth ($\omega_{cutoff} = \frac{2}{\sqrt{LC}}$) in the variable gain distributed amplifier.

The input and output are 50Ω transmission lines to accommodate proper connection to standard testing equipment. However, the intermediary transmission lines, at the interface of the distributed amplifier and the 8-τ section (Z_1) and the interface of the 8-τ section and the trombone line (Z_2) have no such restriction. For a fixed delay resolution or line cutoff frequency, any increase in interstage characteristic impedance causes a decrease in line capacitances, therefore limiting the maximum allowable size of transistors tapping the line. The overall gain of the beamformer of Fig. 1 can then be shown to be independent of interstage impedances. Hence, for simplicity, all lines are 50Ω, which yields 104pH and 41fF of inductance and capacitance, respectively. All signal path subsystems were designed as differential structures to ensure proper grounding and operation at high frequencies. Signal path connections were realized with Coplanar Striplines (CPS) designed with a differential impedance of 100Ω. All transmission lines and on-chip passive components were modeled with IE3D,a method-of-moments based electromagnetic simulator [2].

B. 3-Bit Tapped Delay Trombone Line

The schematic diagram of the tapped delay trombone line is featured in Fig. 2. The trombone structure closely resembles previously reported transversal filters [3]. Unlike those topologies, only one signal path is selected using wideband switches/amplifers for a specific delay setting (e.g. E for 5τ delay). The maximum achievable delay or the desired number of beamformer bits determines the total number of delay sections incorporated in the trombone line. A three-bit trombone structure was chosen because of the unacceptable performance witnessed as the bit count was increased to four. Fig. 3 shows the simulated delay flatness of the shortest path (corresponding to the smallest delay) as the number of bits (or delay sections) are increased. The simulation assumes an ideal switch/amplifier and a quality factor of 10 for on-chip spiral inductors. Thus, the performance degradation is attributed solely to the tapped delay architecture. One can see that the trombone line performance gets better as the number of bits is lowered. A two-bit trombone structure was considered because of its superior performance to its three bit counterpart. However, the penalty in real-estate and system complexity to implement a 4-bit beamformer with a 2-bit trombone design limitation outweighed the tradeoff in performance of a 3-bit solution. For the trombone line, the number of bits implemented, delay resolution and flatness, gain magnitude and flatness, and bandwidth are all crucial performance vectors which must be simultaneously considered during design. The achievable gain of the trombone line[1], to first order, is limited by the unity-gain frequency, f_t, of the technology used for fabrication and the desired delay resolution, τ,

$$A_v = \frac{f_t \pi \tau}{4} \quad (1)$$

Equation 1 indicates that a process with an f_t of roughly 300GHz is required to simultaneously achieve unity gain and a delay resolution of 4ps. Multi-stage amplifiers with bandwidth enhancing techniques are used to achieve a larger gain in a 120GHz process, while maintaining a flat delay response. The circuit schematic of the wideband switch/amplifier is shown in Fig. 4(a). The switch/amplifier is constructed with an emitter follower followed by two differential pairs. Implementing an emitter follower as the first stage of the switch allowed the design to have acceptable input to output isolation in

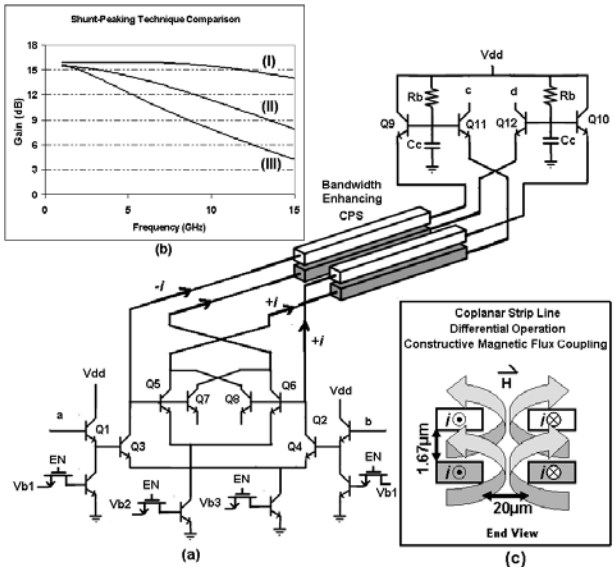

Fig. 4. (a) Wideband switch/amplifier circuit schematic. (b) shunt-peaking comparison; (I) using constructive magnetic coupling in CPS, (II) connection of lower CPS is not inverted with respect to the inner differential pair, (III) no inductor for shunt peaking. (c) end view of bandwidth enhancing CPS during differential operation.

[1]Assuming the wideband switch reflects a dominant pole response.

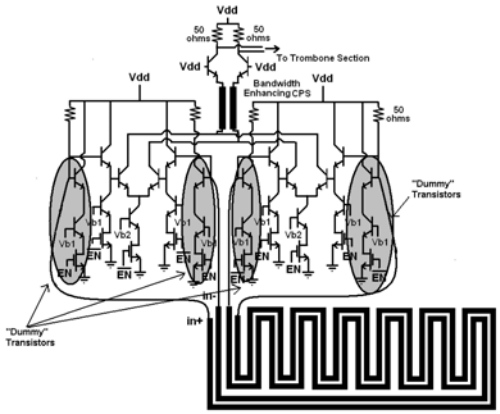

Fig. 5. 8-τ section circuit diagram. EN is the a digit control signal (EN=0:8-τ disabled, EN=1: 8-τ enabled.)

the "off" state and allowed the topology to meet the 41fF input capacitance node limitation. In addition, careful design consideration was taken to minimize delay variation caused by the difference in input capacitance between the "on" and "off" states. After properly sizing transistor junction areas and bias voltages, the impact of switching on performance was minimal.

Various circuit techniques were employed in order to meet the ultra-wide bandwidth requirement while minimizing the delay variation over frequency. Transistors Q7-Q8 with floating emitters extend the bandwidth through differential base-collector capacitance cancelation in a positive feedback configuration, a technique commonly known as neutralization. The amount of neutralization is determined by the device sizes. To ensure system stability, transistors Q7-Q8 are four times smaller than transistors Q5-Q6.

The layout of the trombone line, as well as the 8-τ and distributed amplifier, necessitate a rather long interconnect from the collector terminals of the differential pairs to the emitter terminals of the cascode transistors. If designed judiciously, the interconnect's inductance can provide a shunt-peaking bandwidth enhancement effect by exploiting constructive magnetic coupling as shown in Fig. 4(c). This interconnect is designed as a CPS with a width of 4μm, a spacing of 20μm and a length of 850μm. The connection of the inner differential pair to its CPS is inverted in reference to the outer differential pair. This produces in-phase coupling between all conductors due to the phase inversion introduced by the inner differential pair. This bandwidth enhancement is not seen in common-mode, since the magnetic field lines of the two conductors do not add constructively during common mode operation. Fig. 4(b) shows the simulated effectiveness of the proposed shunt peaking topology based on constructive magnetic coupling.

C. 8-τ Section

This subsection describes the design and implementation of the 8-τ section. The function of the 8-τ section is to provide a frequency-independent 1-bit coarse delay equal to 8 times the delay resolution (32ps). The required delay is achieved through a CPS implemented in the top metal layer. The conductors are of width 10μm and are spaced 10μm apart, resulting in a differential characteristic impedance of 100Ω. The CPS length required for 32ps delay is 4.9mm. The required length of CPS was bent to save chip area, as shown in Fig. 5.

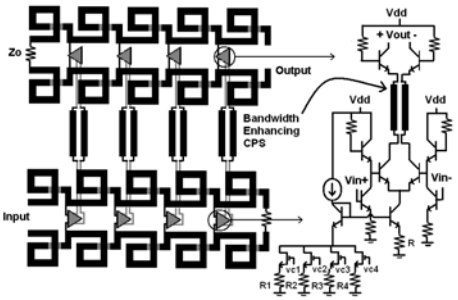

Fig. 6. Distributed Amplifier circuit diagram.

The switching of the delay is achieved through the implementation of two amplifiers, one driven by the input of the CPS, and the other by the output. Each amplifier is fully differential and consists of a common-emitter stage followed by a differential pair. The collector terminals of the inner differential pairs of each amplifier are tied together, and each amplifier can be enabled/disabled through MOSFET switches implemented in series with the tail current sources of each stage, as shown in Fig. 5. Each amplifier also has a set of dummy emitter followers connected to its input in order to present a constant load at the input and the output of the CPS independent of the switch state. Each amplifier also has 50Ω resistors connected to the positive supply rail from its inputs; these provide the required termination to the preceding stage's transmission-line and to the 8-τ CPS.

D. Variable Gain Distributed Amplifier (VGDA)

This section describes the design and implementation of the VGDA. A distributed-amplifier topology was employed to capitalize on its inherent broadband nature in gain and flatness in group delay, which, analogous to the trombone section, results from the fact that the transistor parasitics are absorbed into the lumped transmission lines.

Gain variation is obtained by switching in different degeneration resistors into the current mirror branch. This allows the bias current and hence the gain of the differential pair to be varied. This scheme is illustrated in Fig. 6(a), and allows for four different gain settings in each unit cell of the VGDA. Further, the first and third unit cell are driven by the same set of control voltages, as are the second and fourth. This, along with an appropriate choice of the resistors (R_1-R_4), allows the VGDA to achieve 5dB of gain variation in 1dB steps. In addition to providing variable gain necessary for beamforming, the 5dB gain variation in VGDA can be used to compensate for

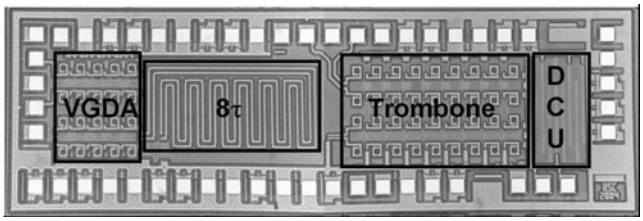

Fig. 7. UWB beamformer chip microphotograph.

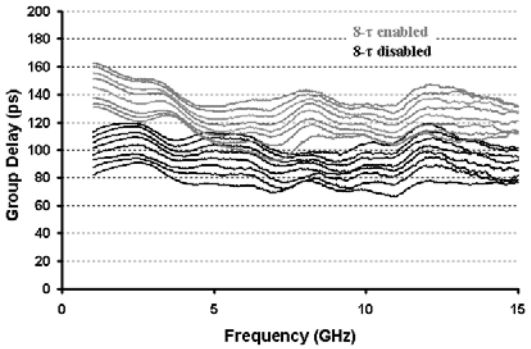

Fig. 8. Measured 4-bit delay variation.

the additional loss associated with the longer paths in trombone structure.

III. Measurement Results

A prototype of the UWB beamformer has been implemented in a SiGe BiCMOS process with 0.18μm minimum channel length for CMOS transistors and maximum cutoff frequency of 120GHz for the HBTs (Fig. 7). The entire chip consumes 0.8mm$\times$2.0mm of silicon area. Although the beamformer is fully differential, single-ended measurements are reported due to the unavailability of UWB single-ended to differential converters in our laboratory at the time of this writing. The 4-bit delay variation for the highest gain setting is shown in Fig. 8, while the controllable gain variation for the lowest delay setting is shown in Fig. 9. Although the controllable delay step (i.e., delay difference) is 4ps, the measured delay in each setting varies across frequency as expected in the tapped delay version of a trombone line (section II, part B). The jump in the delay curves when the 8-τ section is switched in can be attributed to the accumulation of small delay errors in the 3-bit tapped delay trombone line. Fig.10 shows the measurement results of successive tap points in the tapped delay trombone line. In an UWB phased-array system, delay variation causes distortion in the time domain signal. The characterization of this effect is beyond the scope of this paper and will be reported elsewhere [4]. The measured -3dB gain bandwidth is 11.2GHz at the maximum gain setting of 14.2dB. The chip consumes 125mW from a 2.5V supply at the maximum gain setting of 14.7dB.

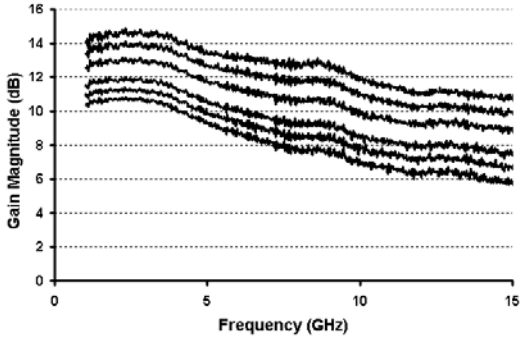

Fig. 9. Measured beamformer controllable gain.

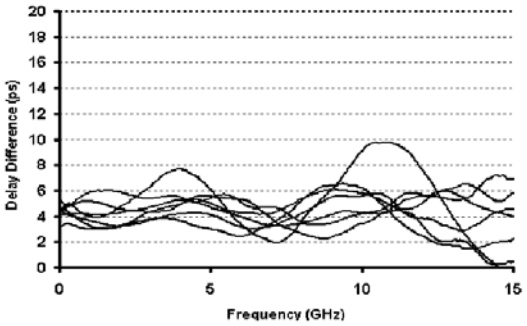

Fig. 10. Measured delay difference of successive tap points in the tapped delay trombone line.

IV. Conclusion

We have demonstrated the possibility of achieving a high resolution UWB beamformer using true time delay variation and gain control in a silicon implementation. The characterization of UWB phased arrays in the presence of circuit imperfections, as witnessed in this work, is still an open problem for future research.

V. Acknowledgment

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