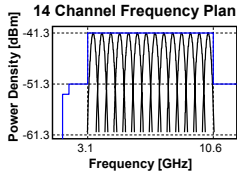


A 3.1-10.6 GHz 100 Mb/s Chipset for Pulsed-UWB

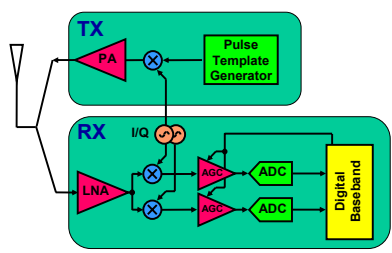
Fred S. Lee, Nathan Ackerman, Manish Bhardwaj, Raul Blazquez, Christian R. Deonier, Brian P. Ginsburg, Johnna Powell, Vivienne Sze, David D. Wentzloff, Anantha P. Chandrakasan

Specifications

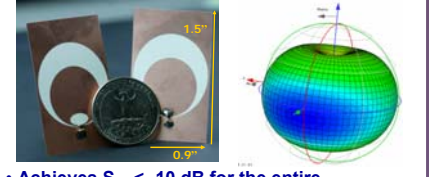


- 500 MHz-wide BPSK Gaussian-shaped pulses
- 100 Mb/s maximum data rate at 10 m
- 14 channels between 3.1 – 10.6 GHz

Block Diagram



Antenna



- Achieves $S_{11} < -10$ dB for the entire 3.1-10.6 GHz range
- Compact, planar design
- Near omni-directional radiation (2 dB gain)

Custom 3.1-10.6 GHz 100Mb/s Chipset

UWB 3.1-10.6 GHz RF Front-End Receiver

Single-to-Differential Converter With Switch-able Notch Filter

- 3-5 dB down-converted NF
- 32 dB avg conversion gain
- -41 dBm input P_{1dB}

3.1-10.6 GHz Un-matched LNA

6-Channel Time-Interleaved Successive Approximation Register (SAR) ADC

SAR has linear scaling of comparators vs. exponential for flash

0.18μm CMOS Dual-ADC Prototype

- Self-timing
- Pre-amplifier duty-cycling
- Full custom dynamic logic
- 7.8mW per ADC

Specifications: 5b, 500MS/s

- Split capacitor array
- Optimized latch strobing
- 6mW, Nyquist performance

3.1-10.6 GHz Pulse Generator

- Pulse Gen.
 - 100MHz PRF
 - BPSK modulation
 - Gaussian shaping
- Pulses simultaneously shaped and mixed to UWB band - BPSK from inverted LO

0.18μm SiGe BiCMOS Pulsed Mixer

Digital Baseband Processor

Trade-off processing energy with QoS
Adapt signal processing to channel quality

MINIMUM POWER OF ECHOS

Energy \propto 1/Threshold

Measurement Results

Chipset Summary

Block	Process	Power [mW]
Transmitter	0.18 μm BiCMOS	31.1
Front-end receiver	0.18 μm BiCMOS	54.3
Dual 500 MS/s ADC	0.18 μm CMOS	7.8
Digital back-end	0.18 μm CMOS	85 (est.)
Commercial PLL		75
Total Power Consumption		253

TX Spectrum Plot

Analog Baseband RX I/Q Signals

Digitized RX I/Q Signals