

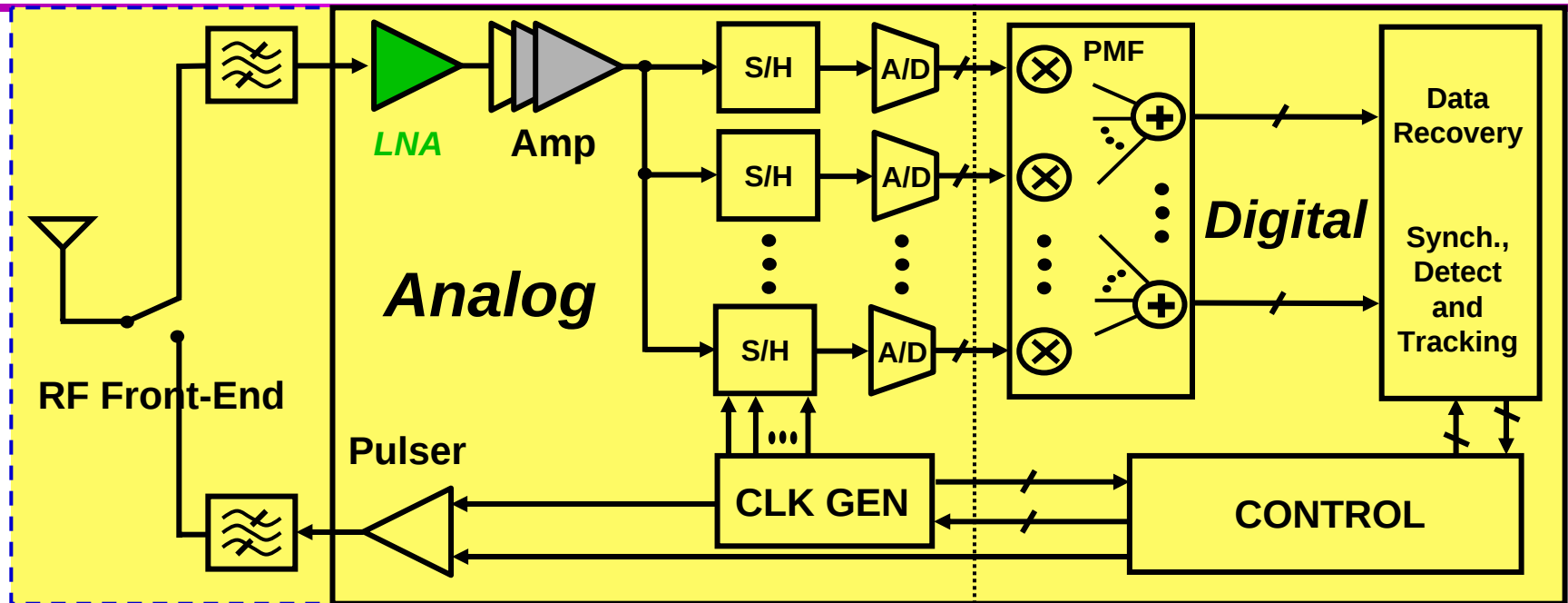
Short Range UWB Radio Systems

*Finding the power/area limits of
CMOS...*



Bob Brodersen
Ian O'Donnell
Mike Chen
Stanley Wang

Integrated Impulse Transceiver

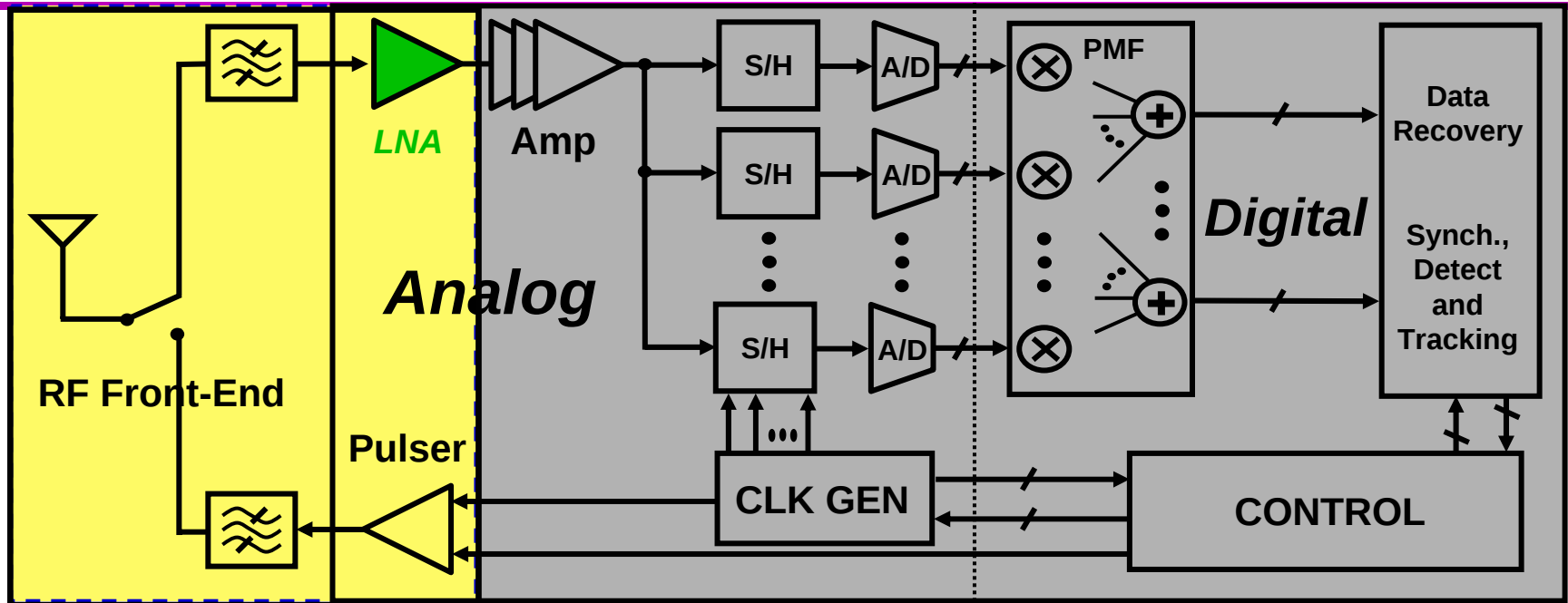


All-CMOS integrated UWB transceiver
for comm. and ranging/locationing
Aggressive low-power design
“Mostly-digital” approach, simplify analog
front-end

Specifications:

- 100kbps over 10m with 10^{-3} BER
- 1mW total (TX+RX) power consumption
- 0-1GHz bandwidth

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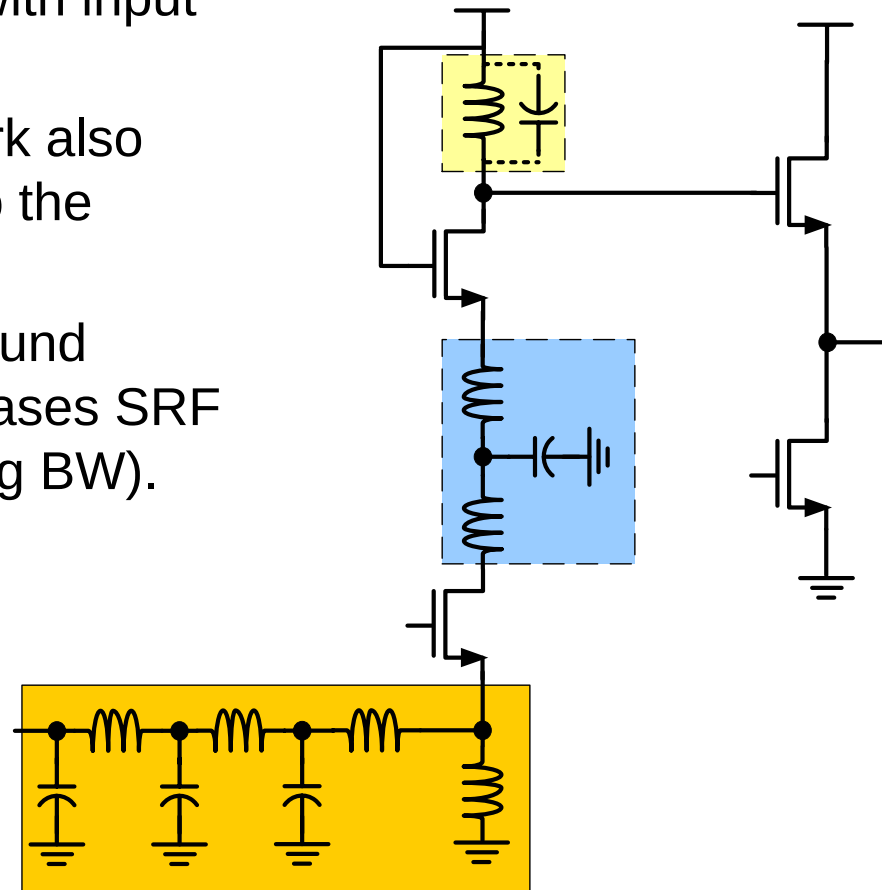
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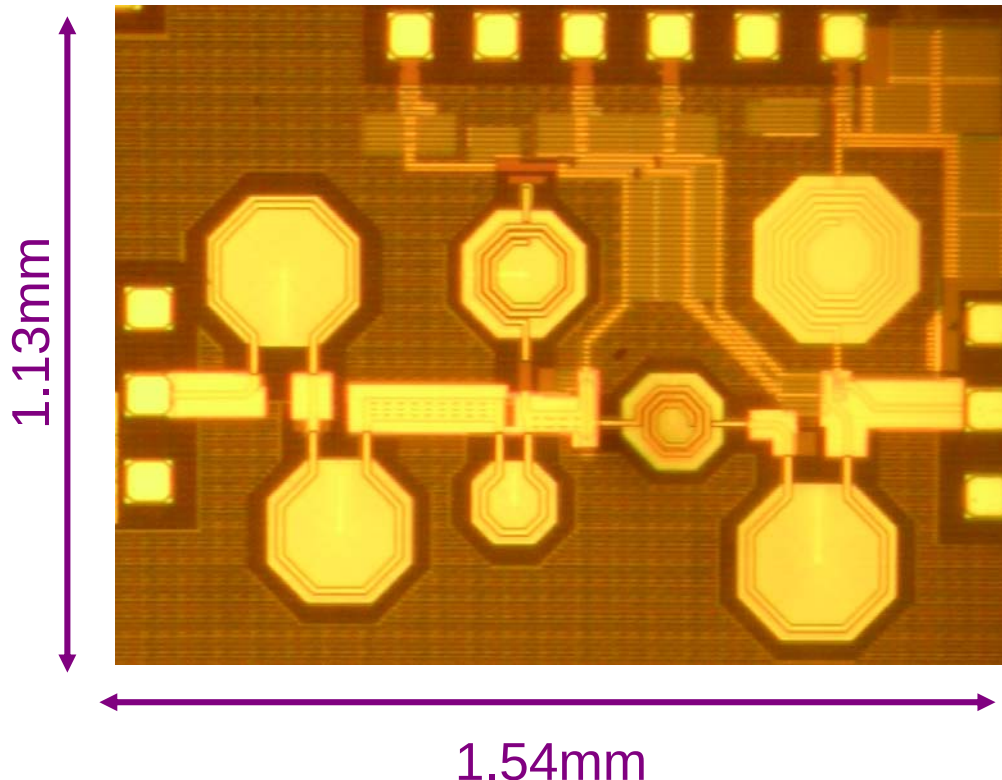
3-10 GHz UWB CMOS LNA (Stanley Wang)

- Common-gate input stage with input matching
- Inter-stage matching network also provides current gain due to the impedance mismatch
- All inductors are pattern ground shielded, except L_{load} . Increases SRF and decreases Q (increasing BW).
- .13 micron technology
- 14 mW, 1 mm²



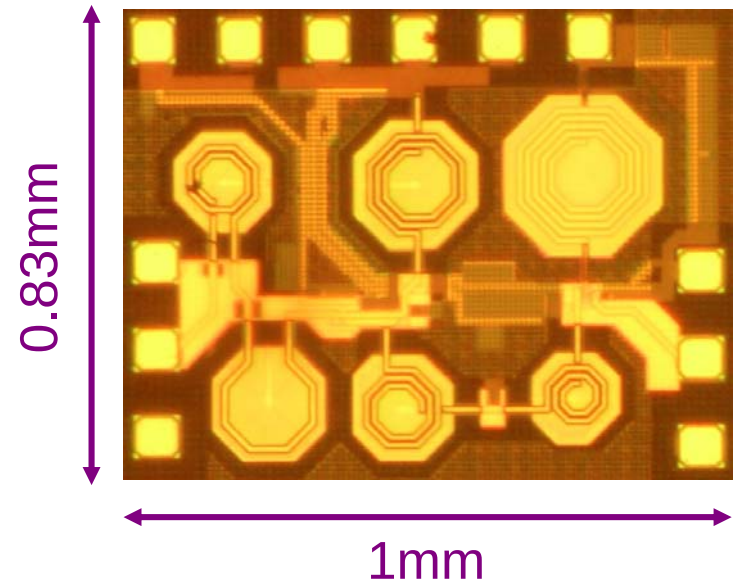
Layout sensitivity

- 3-stage input matching
- “Conservative” layout strategy
 - Keep distance between L's
 - Single-turn inductors

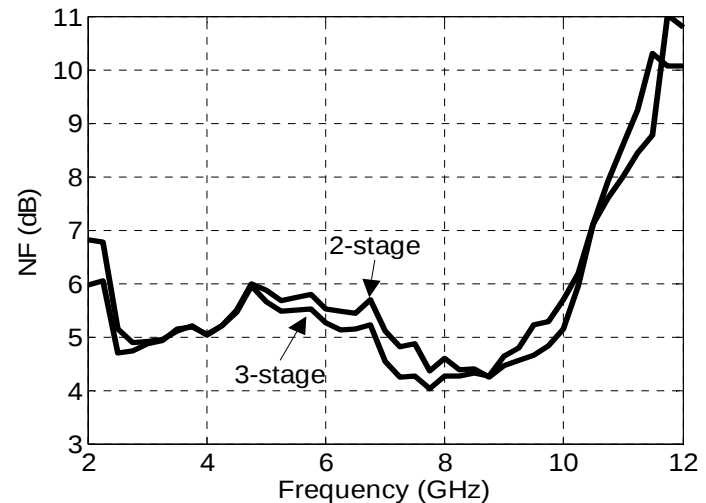
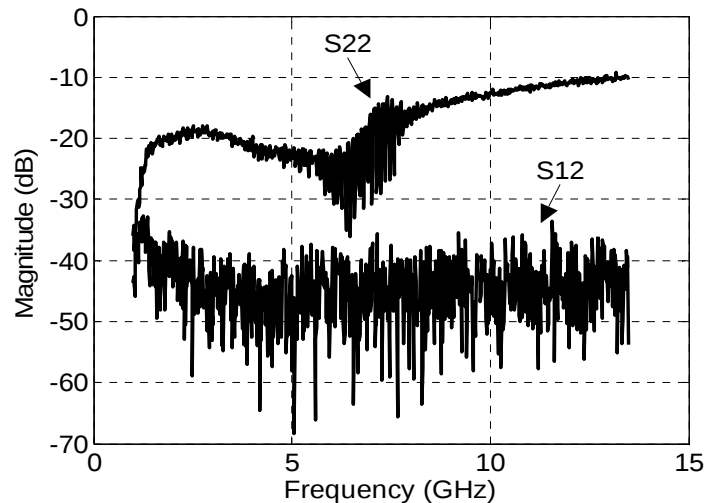
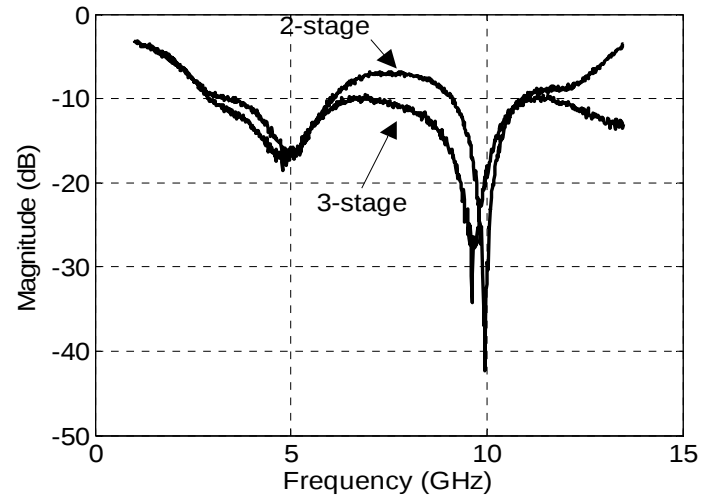
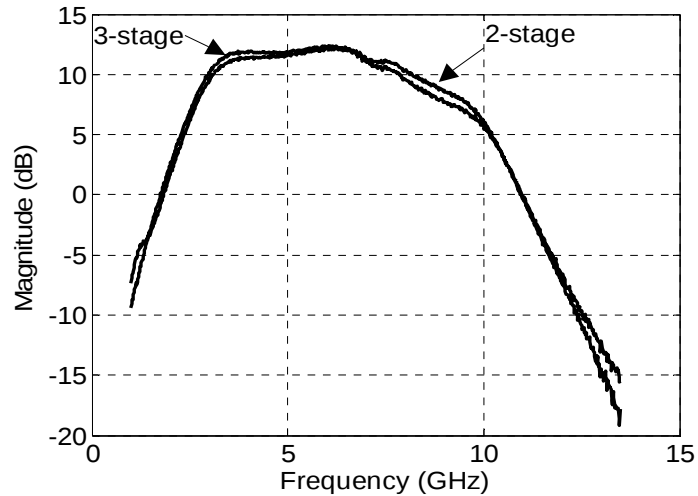


Berkeley Wireless Research Center

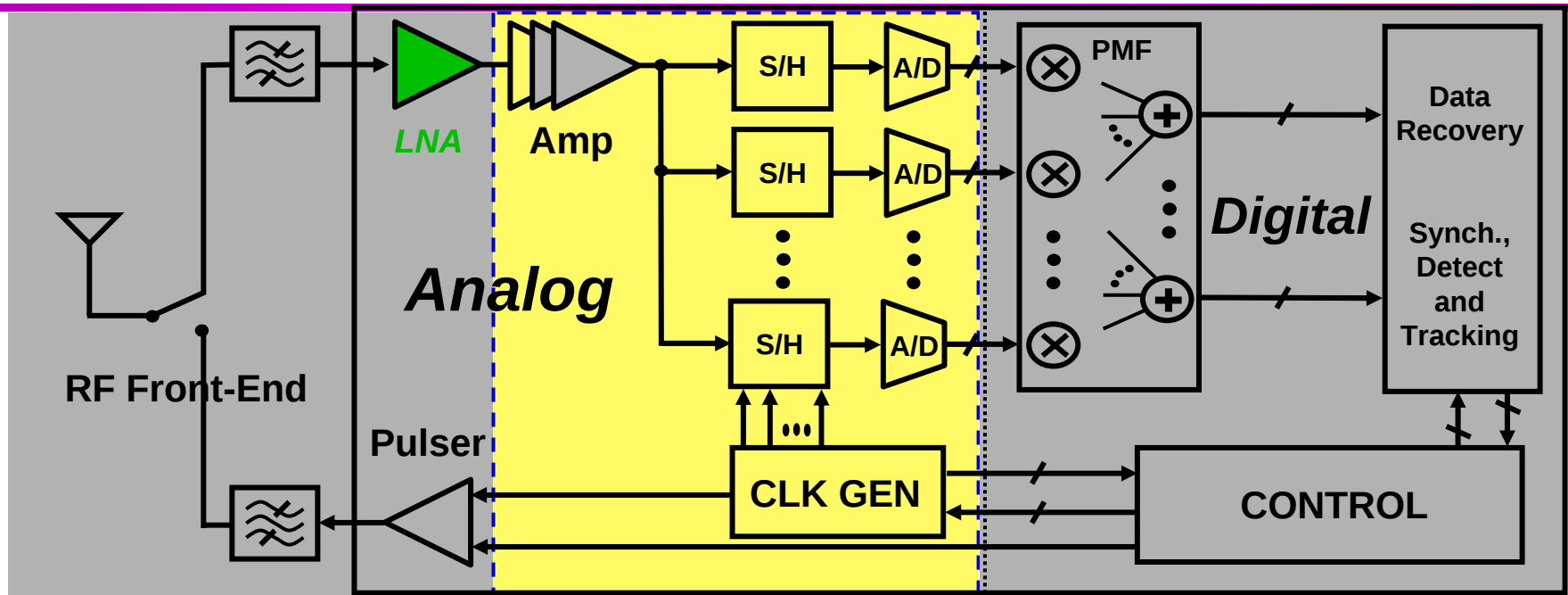
- 2-stage input matching
- “Aggressive” layout strategy



Measurement Results



Integrated Impulse Transceiver



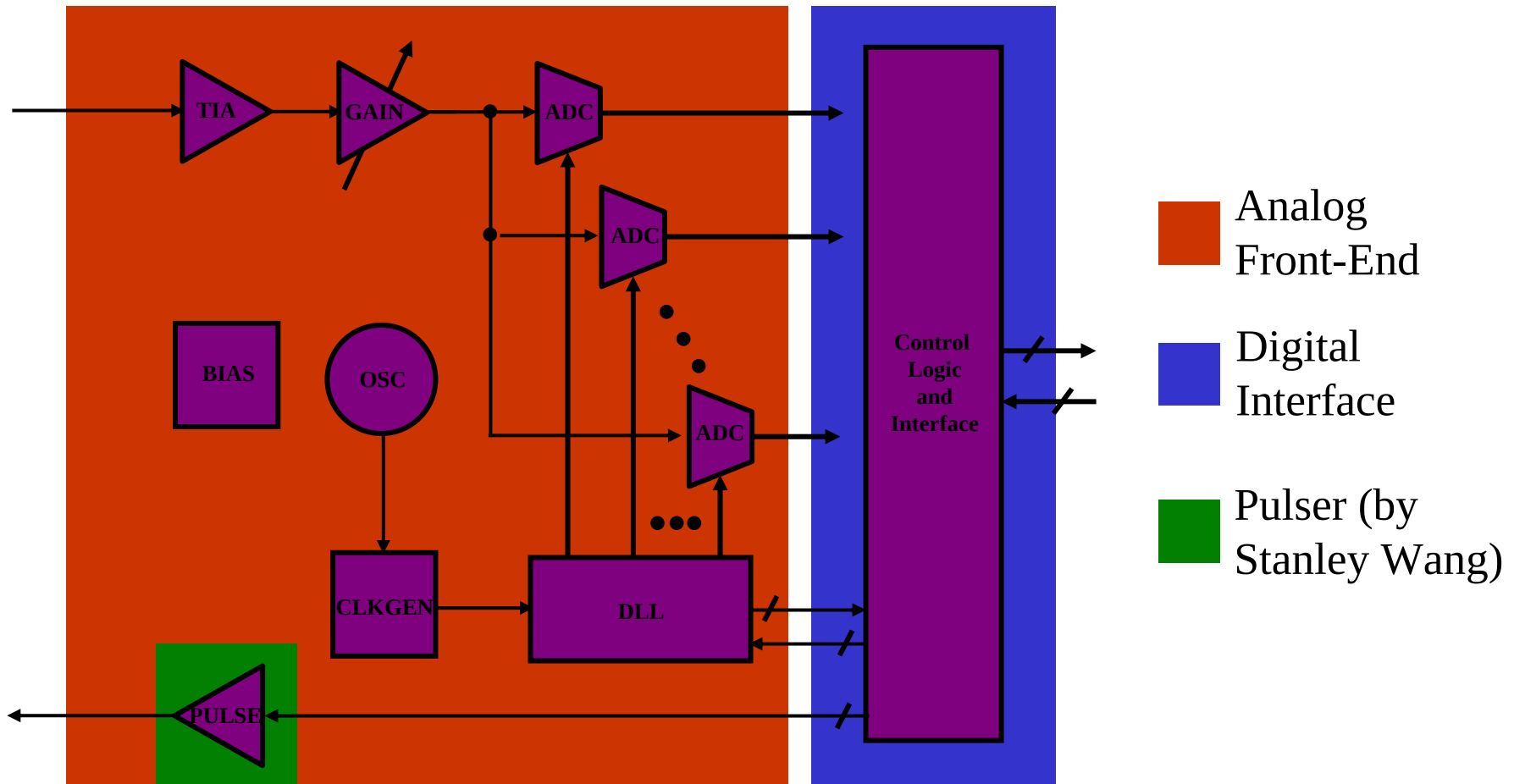
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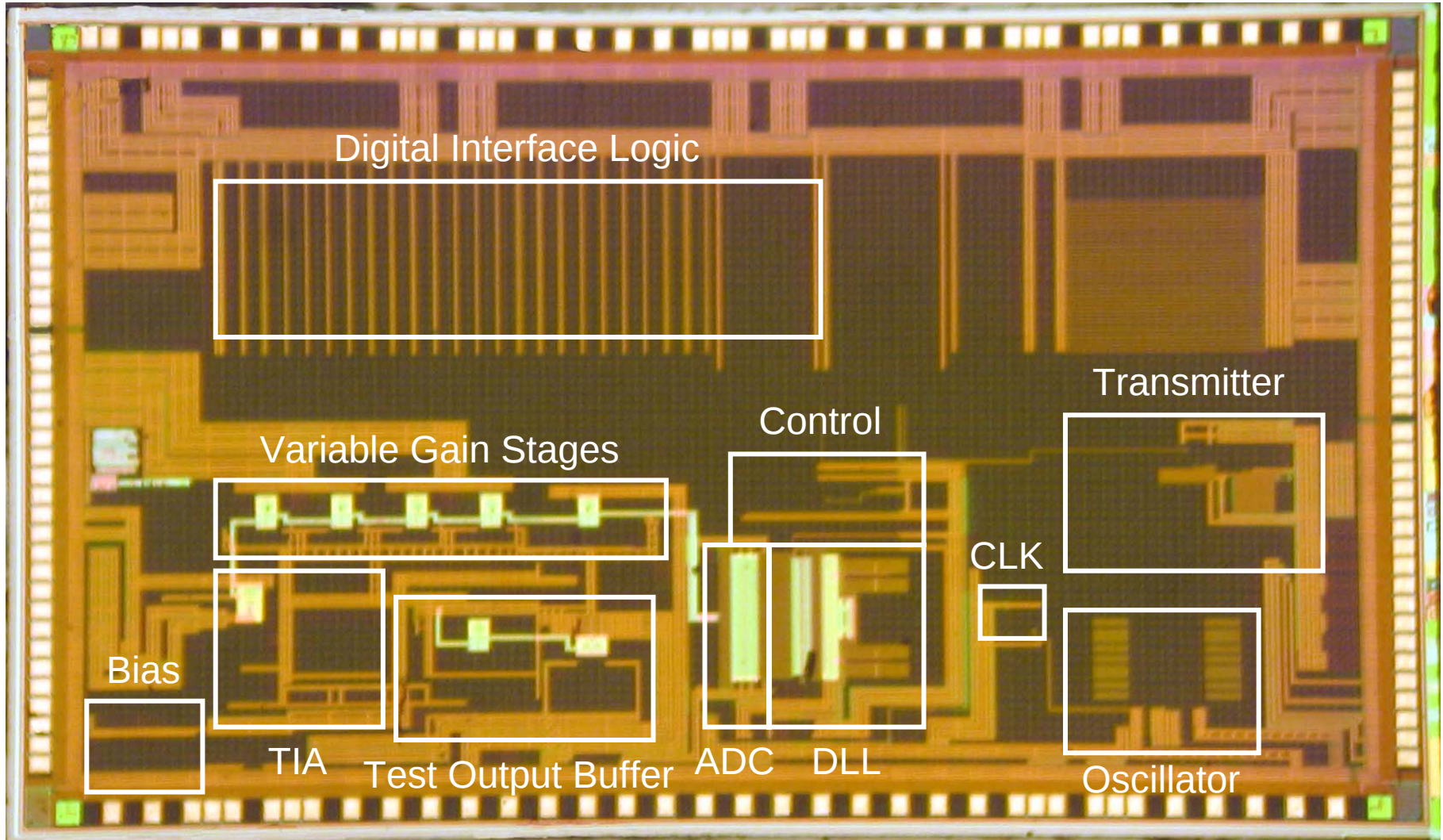
UWB Transceiver Prototype

Based on Digital Sampling/Acquisition Oscilloscopes

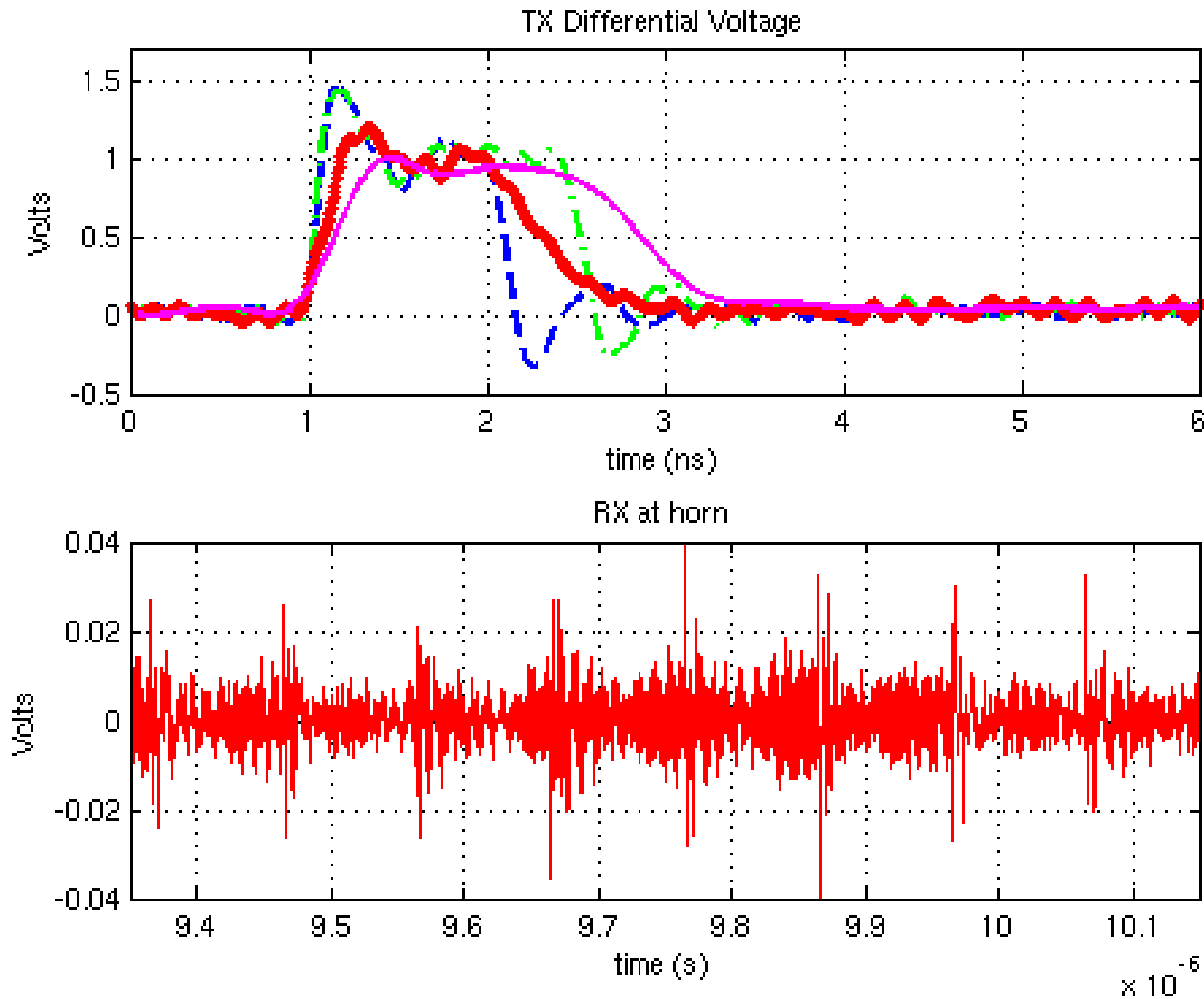


The Integrated implementation...

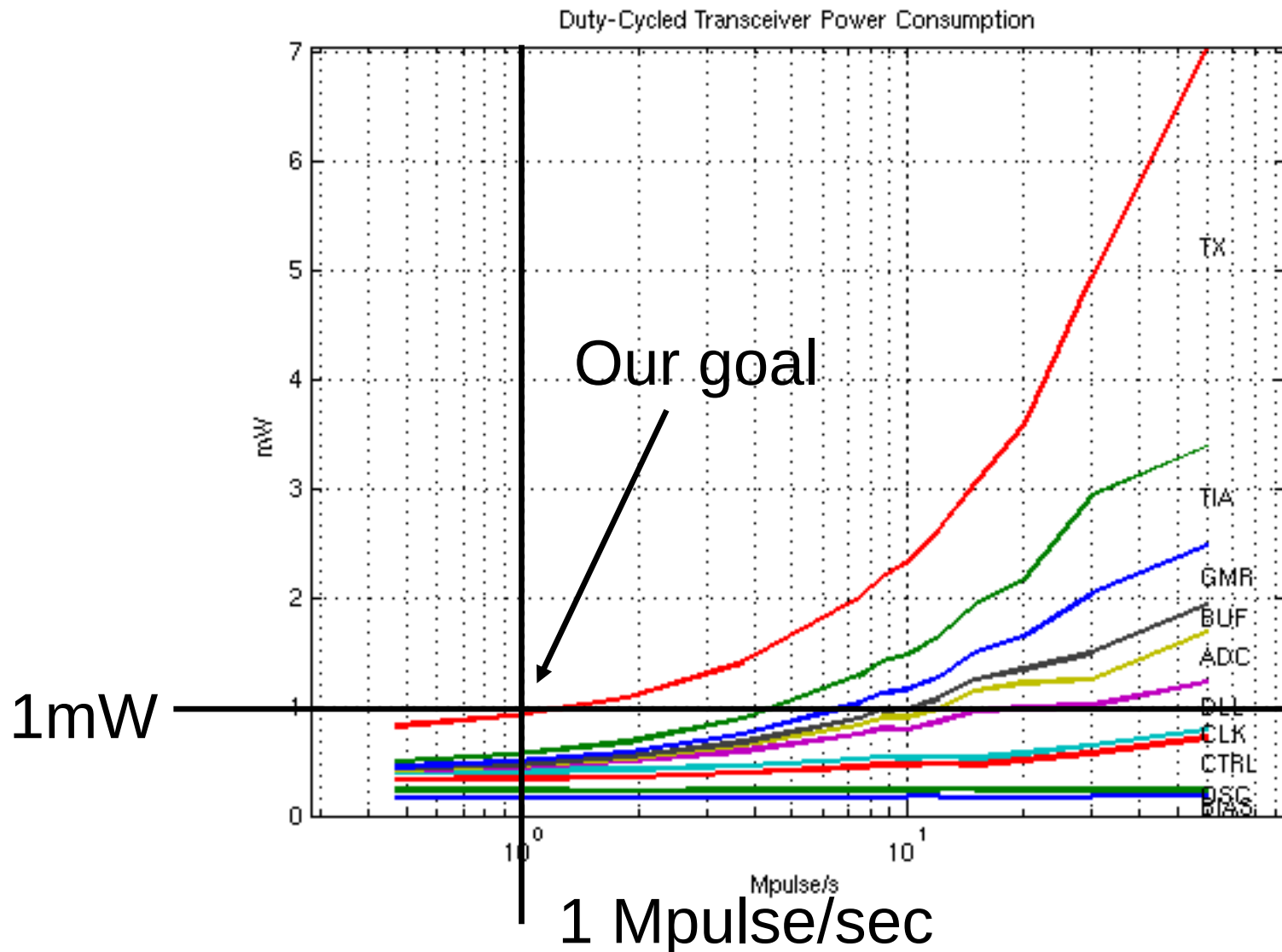
2.8 x 4.7 mm² (13.2 mm²)



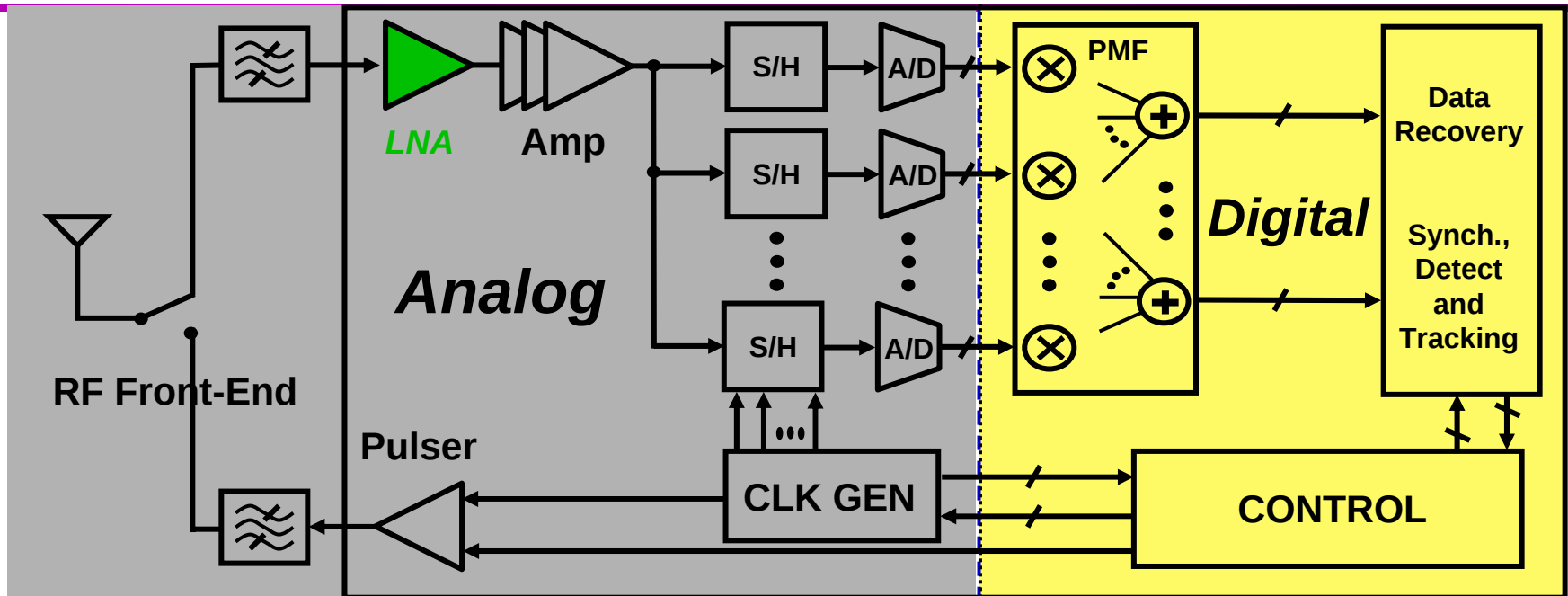
Pulse Transmission & Reception



Variable pulse rate power consumption (2 Gsample/sec sample rate)



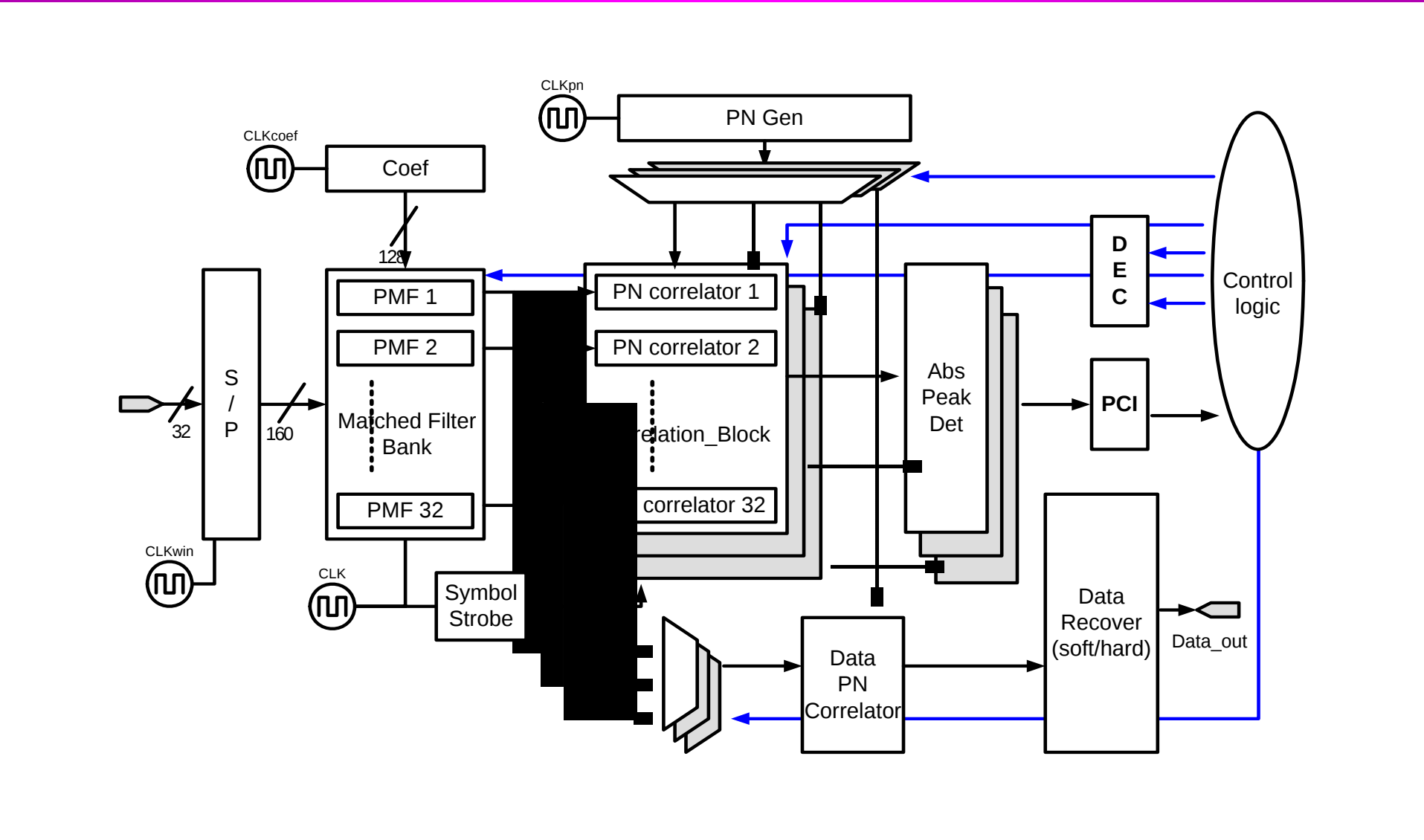
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UWB Baseband Chip

Process: 0.13 μ m (ST Microelectronics)

Size: 3.6mm x 3.3mm

Standard Cells: 530,000

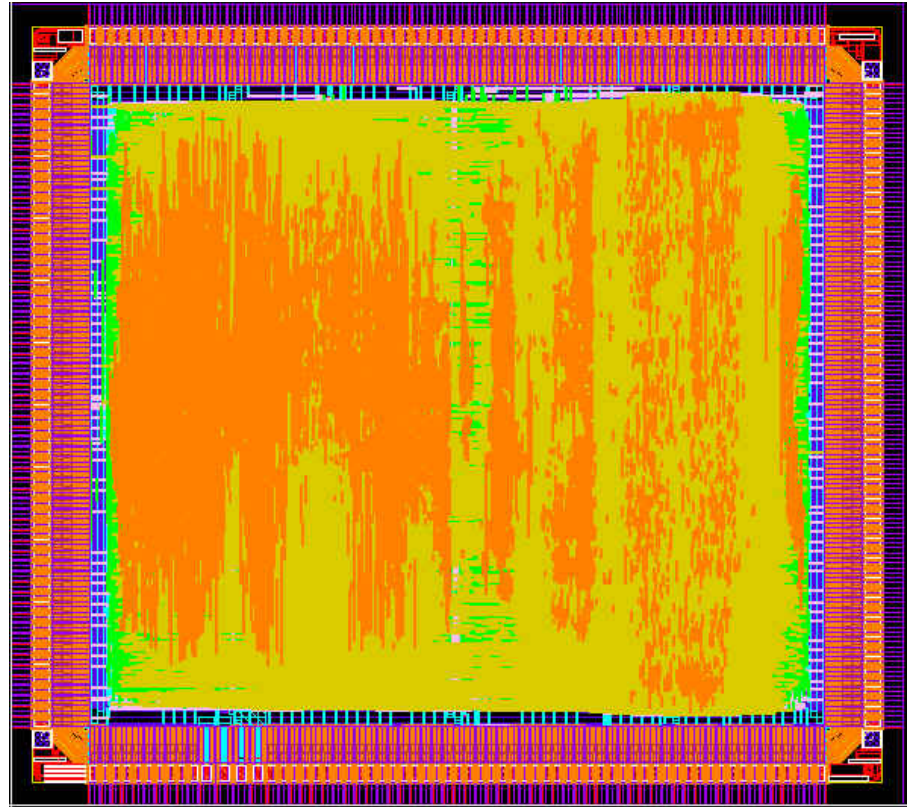
MOPS/mW: 1,500

Power:

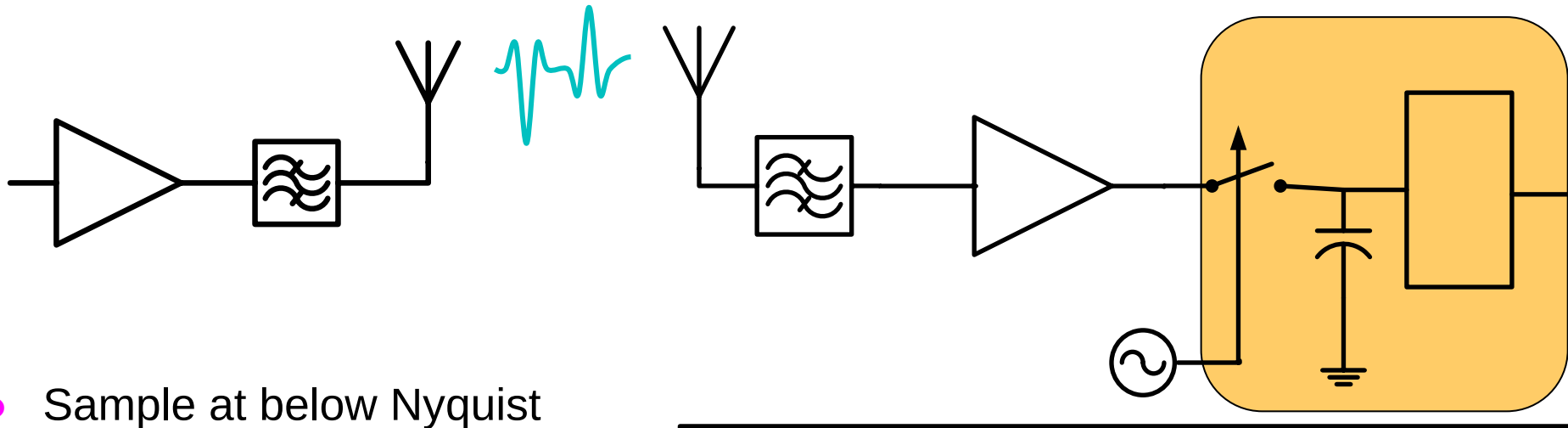
Acquisition $\rightarrow$ 12 mW

Tracking $\rightarrow$ 1.5 mW

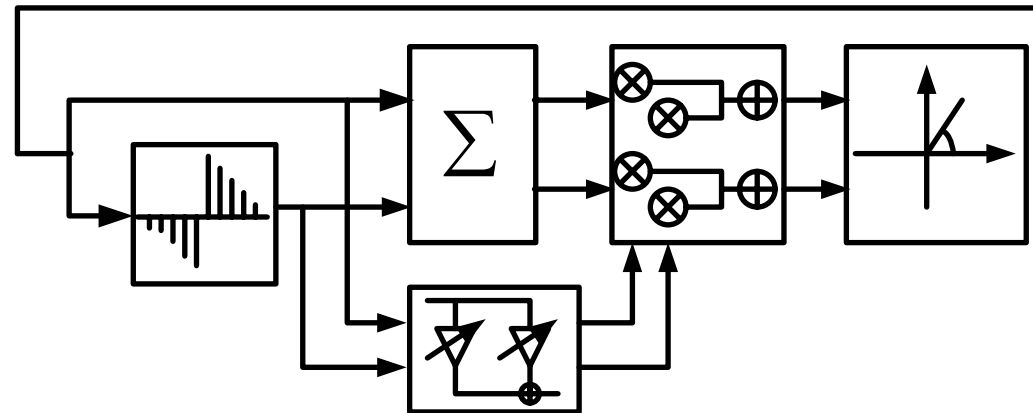
@ 1.08 V, 10 MHz clk



3-10 GHz Transceiver Analytic and Sub-sampling for Impulse Processing (Mike Chen)



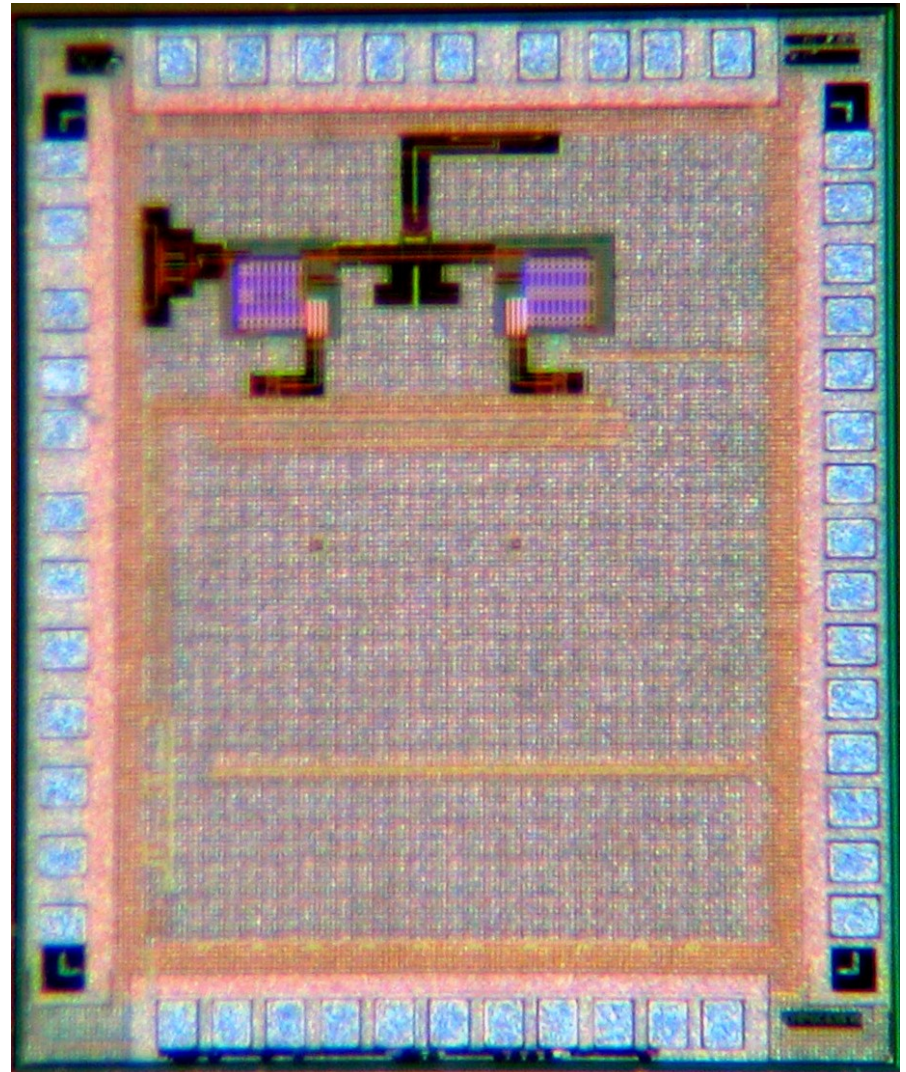
- Sample at below Nyquist
- Analytic signaling reduces the sensitivity to timing offsets
- Provides fine timing resolution
- Mostly digital solution
- **A/D is critical component**



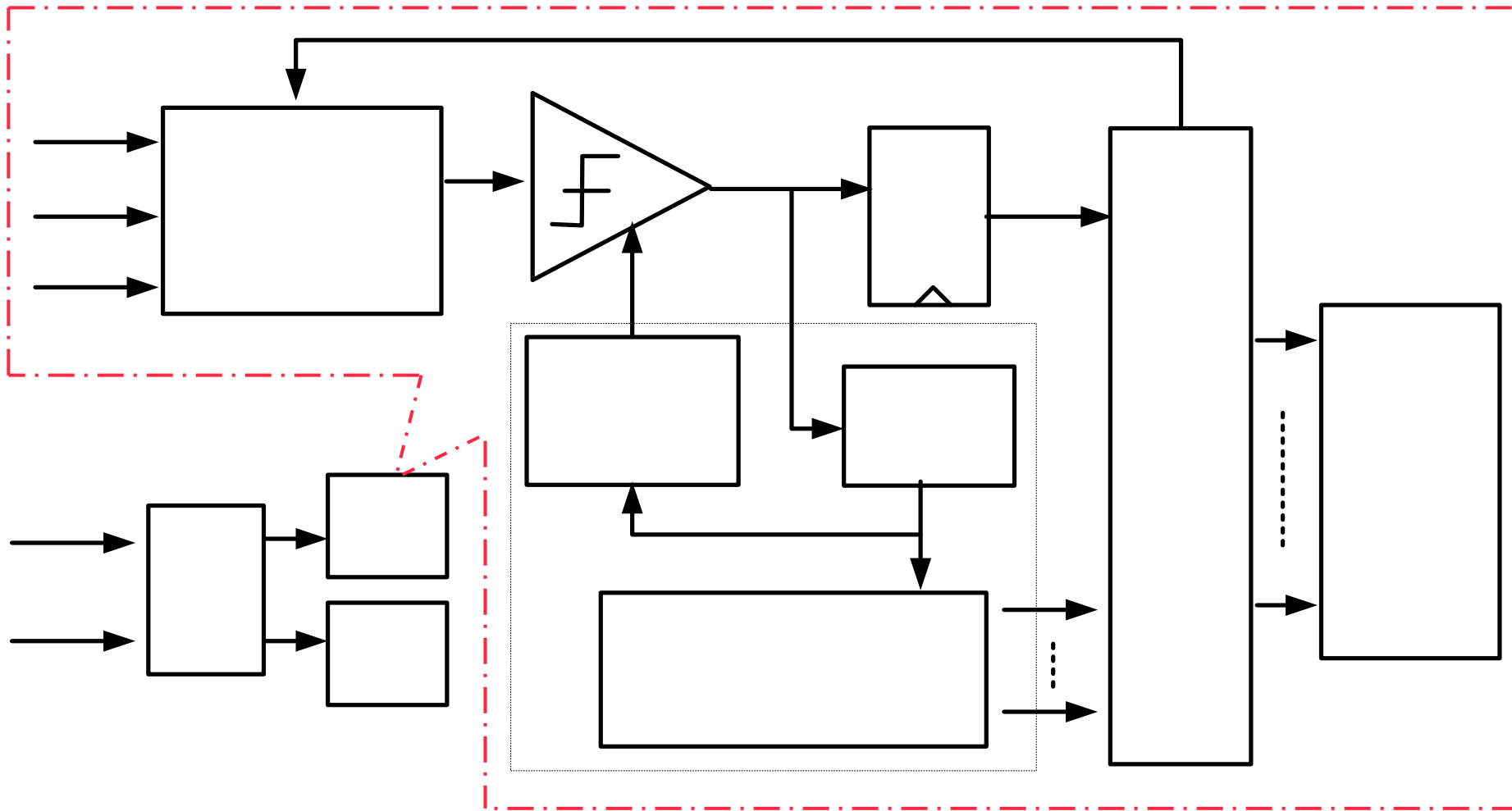
Asynchronous ADC prototype

Highlights:

- Asynchronous SAR ADC architecture to meet speed requirement
- 600 Msamples/Sec, 6 bits 5 mW, .12 mm²!!
- Input 3dB bandwidth > 4GHz
 - Sub-sampling RF
 - 8 Gigasamples/sec < 100mW

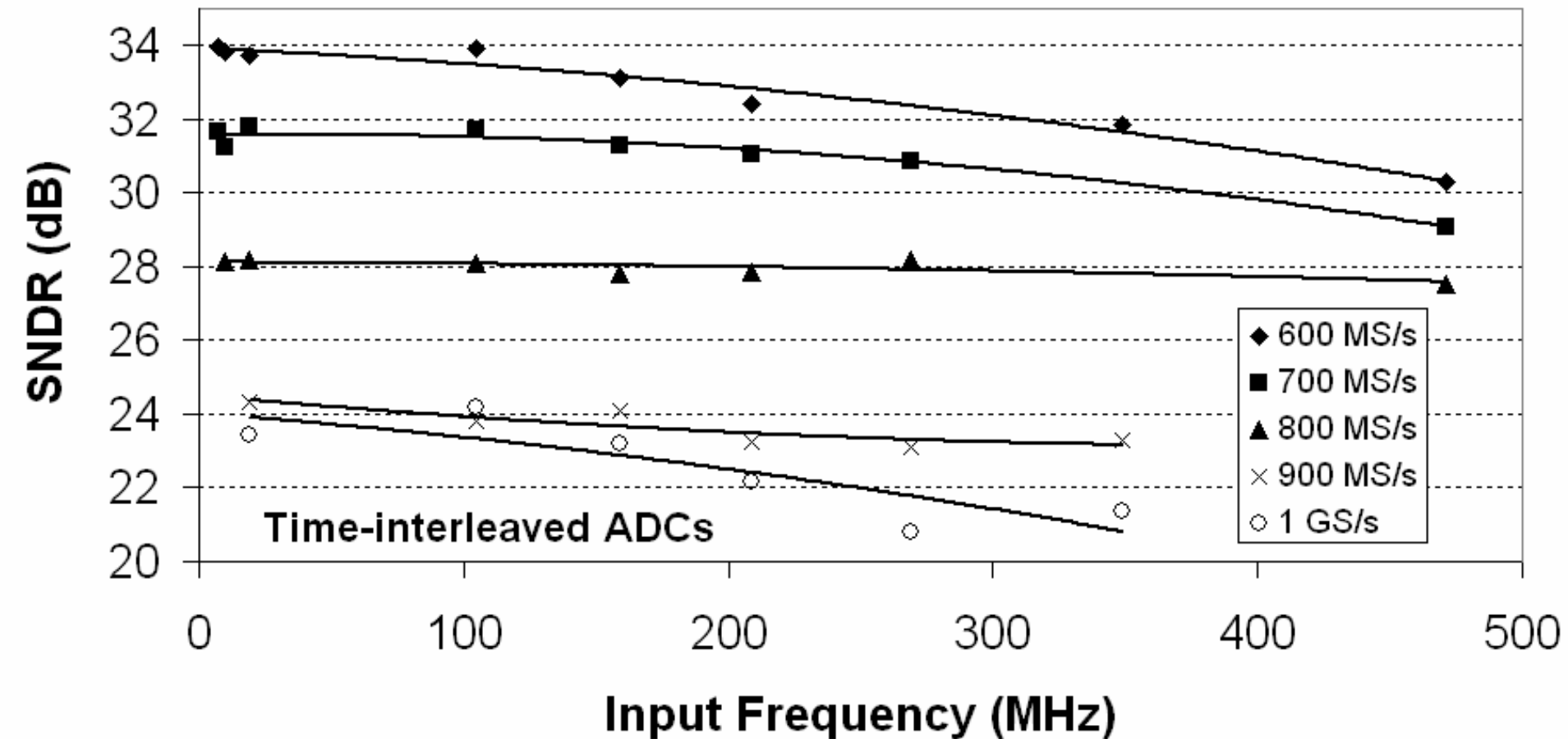


Time-interleaved 2X Async. ADC



No clock higher than the sampling frequency

A/D Performance



Demonstrated .13 Micron CMOS capabilities

- 10 GHz LNA - at 10 mW and 1mm²
- Impulse transceiver at 1 Megapulse/mW
- DSP baseband at 1.5 GigaOps/mW
- A/D at 600 Msamples/sec, 6 bit @ 5mW, .12mm²

Even more important is that these numbers will improve with scaling of the technology....