

# AN INTEGRATED, LOW POWER, ULTRA-WIDEBAND TRANSCEIVER ARCHITECTURE FOR LOW-RATE, INDOOR WIRELESS SYSTEMS

*Ian D. O'Donnell, Mike S. W. Chen, Stanley B. T. Wang, Robert W. Brodersen*

Department of Electrical Engineering and Computer Science  
University of California, Berkeley  
Berkeley, CA 94720  
{ian, swchen, sbtwang, rb}@eecs.berkeley.edu

## ABSTRACT

This paper describes the system architecture and circuit design constraints for a proposed Ultra-Wideband radio transceiver. Targeting a sensor network application, the radio supports peer-to-peer communication at greater than 100kbps over 5 meters with a 1mW total (TX+RX) power budget. A narrow pulse (approximately 1ns wide) is transmitted using simple digital switches; spreading the energy over a Gigahertz of bandwidth. Reception, after gain and filtering, occurs in a bank of A/D converters which capture the received pulse in an adjustable window of 16 to 64ns. This window is composed of 32 to 128 data samples at a 2GHz rate and is repeated at the pulse broadcast frequency which may range from 62.5MHz to 1MHz. The implementation issues of this system, including clock generation, conversion bit-widths, gain, and the choice of pulse rate versus pulse amplitude will be discussed along with the subject of interference and the idea of “imperceptible” operation.

## 1. INTRODUCTION

The FCC has recently approved the use of Ultra-Wideband technology, allowing deployment primarily in the frequency band from 3.1GHz to 10GHz, but also below 960MHz for imaging applications, at power levels similar to Part 15 [1]. Ultra-Wideband (UWB) radios communicate with short pulses or cycles on the order of nanoseconds, spreading their energy over a wide swath of bandwidth, as opposed to modulated sinusoids whose energy is localized around a single frequency. A sample pulse is shown in Figure 1 below.

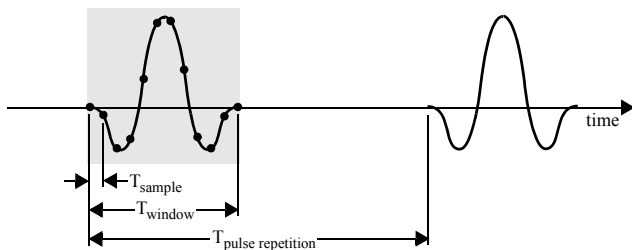


Figure 1. Example Received UWB Impulse

Owing to its unlicensed use, and prospect for large bandwidths and hence large data rates, interest in UWB has been very high. In addition, due to the simplified analog front-end, and duty-cycling nature of pulse-based communication, this approach promises much lower power consumption and higher integration than might be conventionally feasible. However, concern has been growing that the interference generated by the presence of dozens or hundreds of UWB radios, even at Part 15 levels, will swamp out existing narrowband systems.

Because interference is such a main concern, one goal of this research is to explore the feasibility of “imperceptible” operation; setting the power spectral density at three meters to be roughly equivalent to the background thermal noise. Simulations indicate that reasonable throughput, on the order of 100kb/s to 1Mb/s, is still obtained in this situation. These performance levels seem well-suited to an indoor wireless sensor network, where short distances, lower bit-rates, and low power consumption are required.

Recently there has been a burst of activity in Ultra-Wideband and some notable publications of UWB systems may be found in references [2], [3], [4], [5], [6], and [7]. While a number of different architectures are discussed, the issues of circuit constraints for an integrated ASIC design and the effect of limited transmit power generally are not found, but will be discussed here.

## 2. PROPOSED ARCHITECTURE

Based on a “mostly digital” conception, the proposed architecture consists of a simple baseband analog section followed by a larger digital processing backend. We attempted to bring the digital logic as close to the antennas as possible to gain the benefits of robustness, flexibility, scalability and low power operation. The receiver is based on a digital matched filter, which is optimal for baseband pulse reception in the presence of white noise [8]. Even in the presence of colored noise or narrowband interferers an FIR filter structure can approximate the optimal response.

One goal of this architecture is to provide adequate flexibility for further experimentation. Towards that end, the trans-

mitter circuit and receiver LNA need to be designed with the ability to support different antennas (i.e voltage driven versus current driven) and hence different antenna impedances. In addition, the matched filter coefficients and spreading-gain sequences were kept fully programmable. The design also supports variable transmit power levels and pulse repetition frequencies. While the transmitter is able to generate both 2-PAM and 2-PPM modulations, for the sake of simplicity [9] the receiver currently only implements 2-PAM reception.

As the received energy from an impulse is localized in time to around the channel delay spread, the receiver need be concerned with only a relatively narrow window of time. To meet the Nyquist criterion, this window must be sampled at a high rate, viz. twice the highest frequency of the pulse that still contains significant energy. Hence, depending upon the pulse repetition rate, the receiver frontend may be turned off during the interval between expected pulses to save power.

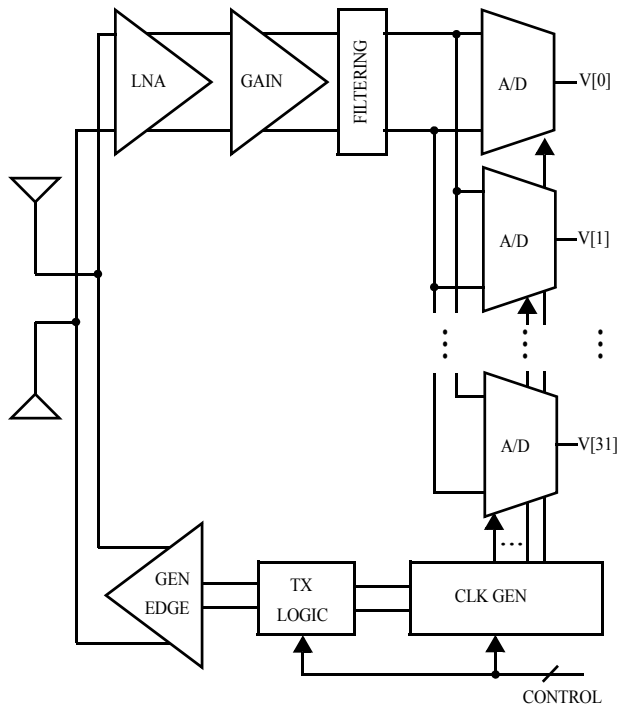


Figure 2. Analog Frontend Block Diagram

In the analog frontend, shown above in Figure 2, reception consists of gain and filtering followed by sampling. Transmission is achieved with a bank of parallel inverters; by changing the transmitter supply voltage and the effective width a variety of driving strengths may be obtained. All of the analog circuits are designed differentially to combat digital switching noise that is expected to couple into the circuitry. This comes at the expense of higher power

consumption, but renders the digital spikes, which could easily corrupt the pulse reception, to common-mode. Also, all of the receive gain stages are designed to be turned on and off quickly to save power through duty-cycling. Because these gain stages are wideband, the dominant time constant is small, on the order of a nanosecond or less, which makes for fast settling during these transitions. Also, the amplifiers are designed for fast overload recovery, so that large signals do not saturate the frontend. The LNA is designed for impedance matching over a range of values to allow for different antennas to be used.

At these frequencies (DC to 1GHz) it is difficult to design an UWB antenna that is physically small with low dispersion and high radiation efficiency. Good candidates for such an antenna are the Large Current Radiator, a low impedance, current-mode antenna; and the terminated dipole, a higher impedance, voltage-mode antenna [11]. As the design of an ultra-wideband matching network may be difficult, two LNA's may be designed for these two impedance extremes if one cannot be made with enough input variation to support them both.

After the LNA, several stages of gain and filtering follow. The filtering attenuates interferers, in particular the cell-phone band around 900MHz, and FM radio and most VHF TV signals below 110MHz. Ultra-Wideband cannot escape having in-band interferers, so it is beneficial to lessen their impact, if possible.

Sampling is achieved with a bank of A/D's operating at the window rate, 62.5MHz. While a single A/D could be designed to run at 2GHz to sample the signal, power may be saved by running smaller sized A/D's at a lower rate. The sampling clocks are generated from a DLL-based clock generation circuit, derived from the system oscillator running at the window rate. After sampling, the bits are aggregated into a larger block of samples and passed to the digital section shown in Figure 3.

Data from the frontend enters the digital backend parallel to parallel convertor which aggregates several consecutive windows of data samples into a block of up to 256 samples. To speed acquisition, 128 samples are searched in parallel by 128 matched filters. To guarantee that a pulse doesn't straddle the boundary between steps, 256 samples are needed. The pulse-matched filters are of length 128 samples (64ns), sized relative to the expected delay spread for an UWB indoor channel[10]. The matched filter outputs are then sent to either an acquisition or synchronization block. For synchronization, as only three values, 'early,' 'on-time' or 'sync,' and 'late,' are needed, all of the other matched filter inputs are disabled to save power. For acquisition, we search over all 128 samples and 11 spreading code phases at

a time as a compromise between area and search time. Once a correlation peak above the programmable threshold is found by the peak detector logic, the backend switches from acquisition to tracking mode. Because 2-PAM is used, the data recovery block is a simple slicer based on a programmable threshold. In the interest of flexibility, two different spreading sequences may be used: one for acquisition and one while synchronized. Both sequences may be of length 1 to 1024.

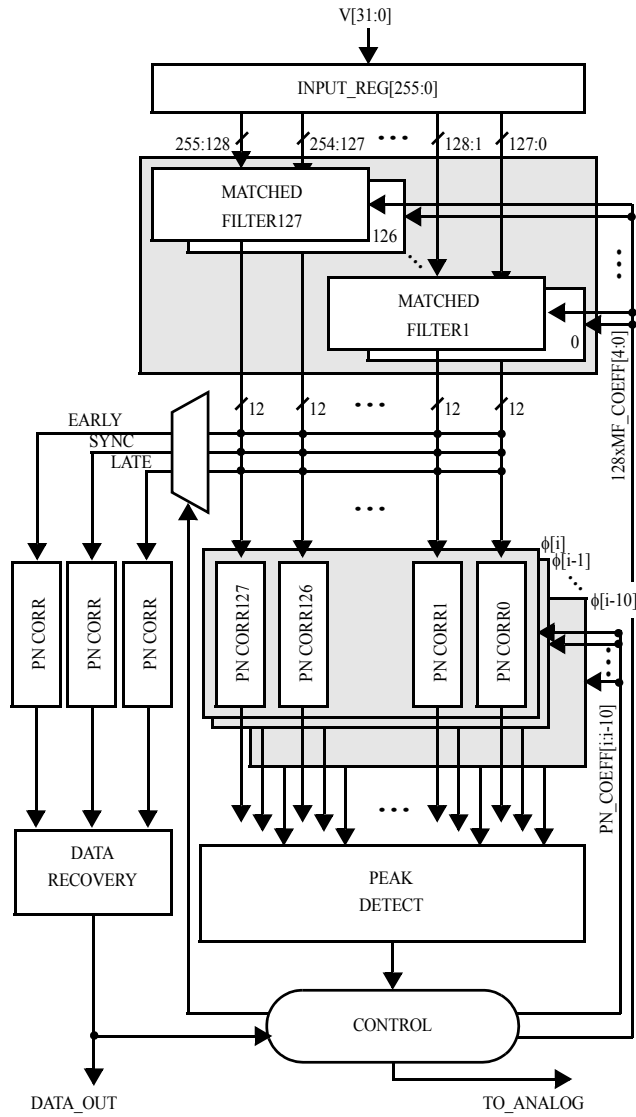


Figure 3. Digital Backend Block Diagram

### 3. SYSTEM SNIR

In the interest of specifying the A/D and matched filter bit-widths, the ‘Signal to Noise + Interference Ratio’ (SNIR) at the matched filter output is calculated per pulse; taking into account limited gain, quantization noise, input-referred

noise figure, and the effect of narrowband interferers. The result of that calculation follows:

Defining the sampled, received signal after the A/D as:

$$V = S + N + I + X$$

where  $S$  is  $K$  samples of the desired pulse; equal to the received pulse after gain and filtering:

$$S = [s[0] s[1] \dots s[K-1]]$$

and  $N$  is  $K$  samples of Gaussian noise; variance set by the background noise floor times the system power gain and noise factor of the frontend,

$$n[k] = \mathcal{N}(0, A_V^2 \cdot NF \cdot kTBR)$$

and  $I$  is  $K$  samples of the total narrowband interference,

$$I = [i[0] i[1] \dots i[K-1]]$$

where a narrowband interferer is modeled as a sinusoid with the equivalent power and uniform random phase:

$$i[k] = \sum_{n=0}^{N-1} A_n \cos(\omega_n T_{sample} k + \theta_n)$$

and,  $X$  represents the quantization error; assumed to be zero mean and uniform over +/- 1/2 lsb:

$$x[k] = \mathcal{U}(0, \frac{\Delta_{A/D}}{12})$$

Defining the matched filter coefficients as:

$$W = S + Y$$

where  $S$  is again  $K$  samples of the desired pulse, and  $Y$  represents the quantization error for the matched filter coefficients; also assumed to be zero mean and uniform over +/- 1/2 lsb:

$$y[k] = \mathcal{U}(0, \frac{\Delta_{MF}}{12})$$

Then the output of the matched filter,  $Z$  is equal to:

$$Z = V W^t$$

and we may define the SNIR as:

$$SNIR = \frac{E[Z]^2}{E[(Z - E[Z])^2]}$$

because all of the noise is zero mean, so:

$$E[Z] = (\sum \xi^t) = \sum s[k]^2 = P_S$$

Then, SNIR is:

$$\frac{P_S^2}{P_S(\sigma_{NX}^2 + \sigma_Y^2) + (\sum R_{II} \xi^t) + K\sigma_Y^2 \left( \sigma_{NX}^2 + \sum_{n=0}^{N-1} \frac{A_n^2}{2} \right)}$$

where:

$$\sigma_{NX}^2 = \sigma_N^2 + \sigma_X^2$$

and  $R_{II}$  is a  $K \times K$  matrix whose elements are given by

$$r_{II}[i,j] = \left( \sum_{n=0}^{N-1} \frac{A_n^2}{2} \cos(\omega_n T_{sample}(i-j)) \right)$$

for  $i,j = [0, 1, \dots, K-1]$ .

Using this equation, one may explore how many bits are needed in the A/D for a given SNIR per pulse at a given level of interference. The impact of interference at a certain frequency is a function of the shape of the pulse; however, for simplicity, the graph is plotted against the total received interference power.

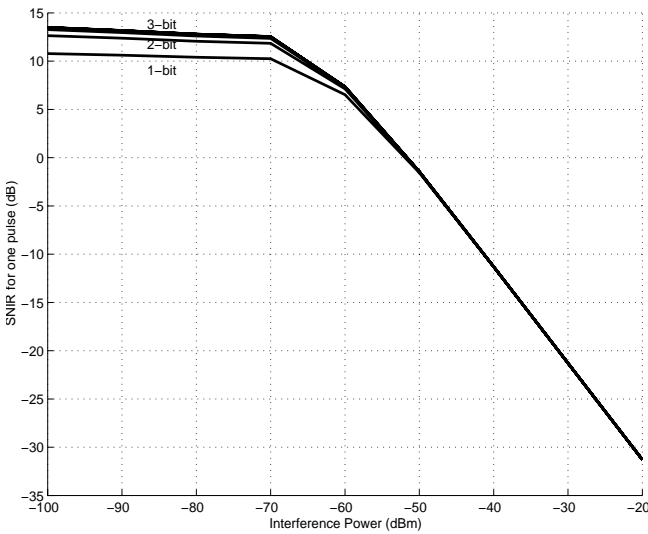


Figure 4. SNIR vs. Interference for A/D Bitwidths

Simulations were run using a gaussian monocycle pulse [2], as depicted in Figure 1, sent at a 10MHz rate, with the received amplitude set such that the power spectral density of the received pulse was roughly equal to that of the thermal noise floor (-174 dBm/Hz). The UWB channel model was for a 3 meter path; derived from an in-house ray-tracing tool which estimates the impulse response using a 3-D indoor building model [13]. A noise figure of 10dB was assumed for the analog frontend, and the gain was fixed at 80dB. Interference was generated based on measurements taken with a spectrum analyzer to represent ‘typical’ levels and scaled over the shown range. Additionally, offset of 10mV was assumed at the input to the A/D.

In Figure 4 we see that, only at low levels of interference where we are noise-dominated, does more than 1 bit in the A/D improve things. As interference increases, the SNIR gets worse and 1 bit is indistinguishable from the other bit-widths (simulations were done to 8 bits.) This realization actually simplifies the analog frontend design and saves power. No automatic gain control (AGC) loop circuitry, such as a peak detect and hold or variable gain amplifier, is necessary.

Given a 1-bit A/D, we now examine the matched filter bit-width requirements (Figure 5).

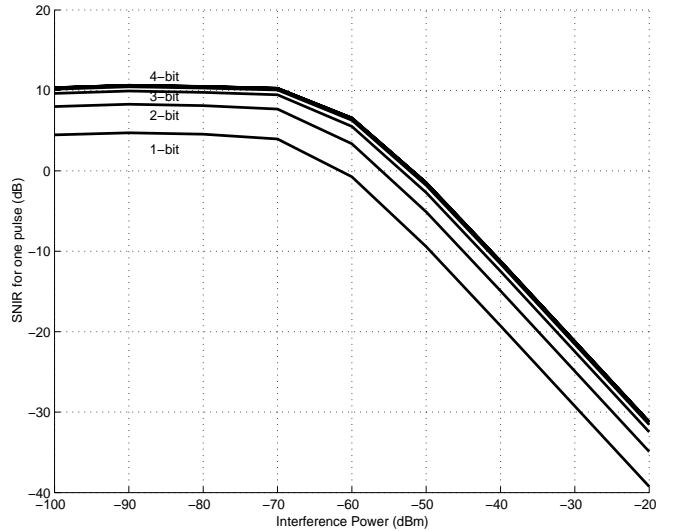


Figure 5. SNIR vs. Interference for MF Bitwidths

In this case we see that a 1-bit matched filter coefficient is not necessarily adequate, as the performance is worse over all levels of interference. Intuitively, the matched filter is correlating against the zero-crossings of the input, so the more accurate our representation of the pulse, the better our estimate becomes. When the A/D input is swamped in noise, the quantization error doesn’t degrade performance much, but the matched filter coefficients need to be fairly accurate.

Based on these curves, it seems a matched filter bitwidth of 5 bits should be more than sufficient. Note that as the full length of our spreading-gain sequence is 1024, which makes -23dB SNIR the lowest supportable value for which we can obtain 7dB; necessary for a  $10^{-3}$  BER target for 2-PAM[8]. This occurs for 5-bits at an input interference power of greater than -30dBm.

#### 4. PULSE RATE CONSIDERATIONS

As aforementioned, a spreading sequence is used to increase the SNIR; however, we have another degree of freedom with an impulse radio: we can directly trade-off pulse rate for pulse amplitude, maintaining the same power spectral density. Recall that the Fourier transform,  $F(\omega)$ , of a pulse,  $A*p(t)$  with Fourier transform  $A*P(\omega)$ , repeated at frequency  $f_{REP}$  is:

$$F(\omega) = 2\pi f_{REP} A P(\omega) \sum_k \delta(\omega - 2\pi f_{REP} k)$$

If we constrain the maximum of  $|F(\omega_{max})|^2$  to be constant to meet the FCC requirement, then  $f_{REP}$  may be traded-off against  $A$ .

As the spreading gain is proportional to the square root of the spreading-gain sequence length, there exists an optimal rate and amplitude for a given SNIR per pulse. Slowing the pulse rate down, while improving the BER, lowers the throughput. Likewise, speeding up beyond the peak lowers the amplitude, requiring a longer sequence for the same BER, thereby lowering throughput.

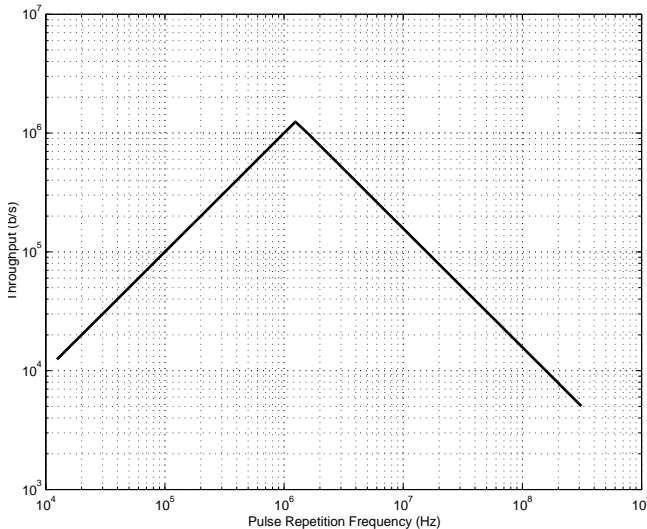


Figure 6. Throughput vs. Pulse Repetition Rate

This ability to trade-off pulse amplitude versus rate with constant bandwidth in order to improve SNIR is characteris-

tic to an impulse UWB system. Using this trade-off, along with conventional spreading gain allows an UWB system to have low impact on existing narrowband users, while still maintaining a reasonable bit-rate. The interference value used in Figure 6 is -40dBm, the average from the spectrum analyzer measurements in our lab. Note that the maximum expected throughput for this case is greater than 1Mbit/s.

#### 5. GAIN AND NOISE CONSIDERATIONS

Ideally, a comparator switches exactly when one input is infinitesimally larger than the other. If we had this level of accuracy, no gain stages would be necessary as we could simply sample the antenna voltage directly. In practice, the offset voltage seen at the input of the comparator will determine the minimum amount of gain necessary to ensure accurate sampling. The worst case situation arises in the absence of interferers with a minimum pulse amplitude that is equal to or less than the noise floor, as this represents the maximum gain scenario for the radio. In such a situation, we can calculate the probability of a comparator error due to offset as:

$$P(Error) = \int P(Error|V_{os})p(V_{os})dV_{os}$$

Assuming  $V_{OS}$  is Gaussian with a mean systematic offset  $\mu_{VOS}$  and variance  $\sigma_{VOS}^2$ , and taking the input as Gaussian, zero mean with variance  $\sigma_N^2$  as in Section 3, we can calculate the probability of a comparator making an error. The exact impact of a comparator error depends on a particular set of  $Y$ , the matched filter coefficients, hence the probability of a sampling error is analyzed for different  $\sigma_N/\sigma_{VOS}$  ratios (neglecting  $\mu_{VOS}$  for the moment.)

$\sigma_N/\sigma_{VOS}$	10	20	33	50	100
p(Error)	3.2%	1.6%	1.0%	0.6%	0.3%

Table 1. Offset Error Probability

Assuming an error rate of 0.01 is acceptable, we can determine the minimum gain necessary relative to the expected offset voltage. Mismatch simulations indicate that simple differential sampling with near minimum sized devices yields offsets on the order of 10's of mV (for 1GHz tracking bandwidth.) Incorporating offset cancellation can bring this number down to several mV. The data in Table 1 implies the input signal to the A/D must be on the order of 33 to 330mV. Assuming the minimum input signal is the voltage noise standard deviation for approximately 1GHz of bandwidth at room temperature on  $50\Omega$ , this corresponds to a minimum gain of about 80dB.

Note that offset arises not only from the comparators, but also from the preceding gain stages. Without the use of offset cancellation techniques and/or capacitive coupling between stages, the systematic offset would swamp the comparators.

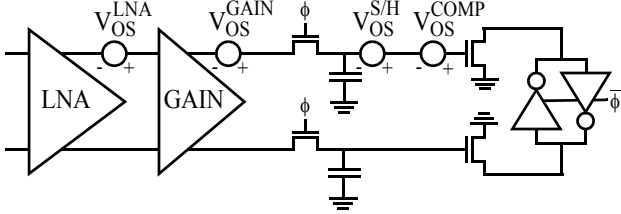


Figure 7. Offset Through the Analog Frontend

If we reexamine the SNIR calculation and add the total offset seen at the comparator input to  $V$  in Section 3, treating the offset as Gaussian with zero mean and variance  $V_{OS}^2$ , we find it appears as additional noise. The variance of the offset voltage will add directly to  $\sigma_{NX}^2$  at the A/D input:

$$\sigma_{NX}^2 = \sigma_N^2 + \sigma_X^2 + \sigma_{VOS}^2$$

The noise figure of the frontend is not critical for design if we assume an interference-dominated channel. Thus, to save power, we may relax the LNA requirement without degrading the overall system significantly. Note that this limits the best achievable performance. The primary LNA design constraint becomes one of impedance matching to the antenna.

## 6. CLOCK GENERATION

Accurate generation of timing signals is another critical aspect of the UWB receiver. Jitter on the A/D sampling operation degrades the pulse SNIR, and any mismatch between the transmit and receive clocks will cause the pulse correlation peak to drift out of the sample window. These mismatch and jitter requirements may be converted into constraints on the oscillator design.

The matching between the transmit and receive clocks must be accurate enough to allow the digital backend to track the drift. In our design the correlation results are compared at the symbol rate, thus requiring the drift over a symbol's reception to be a fraction of a sampling bin to keep the energy within that correlator. Defining  $f_c = 0.5*(f_{RX}+f_{TX})$  and  $\Delta f = |f_{RX}-f_{TX}|$ , we may express this constraint as:

$$\frac{\Delta f}{f_c} \approx \frac{1}{2} f_{symbol} \Delta T_{bin}$$

For the minimum possible symbol rate of the system: 1kHz (1MHz pulse-rate with a length=1000 spreading gain

sequence) the worst-case allowable mismatch  $\Delta f/f_c$  for 100ps is 0.05PPM. This is rather stringent and indicates that for practical matching levels (on the order of several PPM), the slowest system symbol rate allowable will have to be greater than 20kHz. Also, due to this matching accuracy constraint, a crystal-based oscillator will be necessary.

The allowable jitter variance may be approximately mapped to a phase noise requirement for the oscillator[12]. Since the digital backend will track any frequency variations slower than the symbol rate, that is the lower frequency we need to consider. Assuming the mean square phase deviation over a symbol is much less than 1 radian and taking the phase noise spectral density to be of the form:

$$\mathcal{L}(f_m) = \frac{K}{(f_m)^2}$$

Then the corresponding phase noise, given the total accumulated jitter  $\sigma_T$  over  $T_{symbol}$  is:

$$\mathcal{L}(f_m) \approx 2\pi^2 \sigma_T^2 \left\{ \frac{f_c}{f_m} \right\}^2 \frac{1}{T_{symbol}}$$

For an accumulated jitter of 100ps over a 20kHz symbol, we would require -84dBc/Hz at 100kHz for  $f_c=100$ MHz. This level of performance seems achievable, as reference [14] reports a low power oscillator, digitally trimmable to 0.3PPM with phase noise -100dBc at a 100Hz offset.

Given these relationships, we can see that a faster symbol rate would relax the matching constraint as well as help the phase noise requirement. Unfortunately, sending faster symbols may mean less amplitude, if  $f_c$  is held constant, and hence decrease system performance. Likewise, while slowing down the oscillator may help, eventually the sampling clock generation becomes difficult to achieve with low jitter, as the delay line length increases in the DLL (Figure 8).

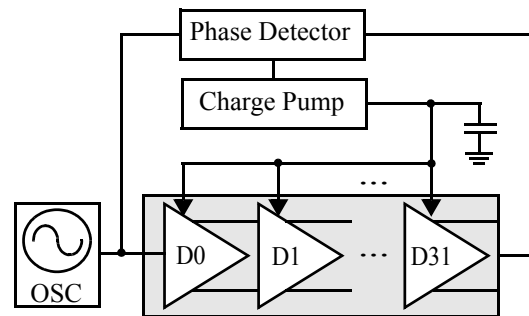


Figure 8. Sampling Edge Generation

A DLL is used to generate sample edges as DLL's do not accumulate jitter [16] and hence have better jitter performance than PLL's. In addition, by choosing the delay line length and  $f_c$  appropriately, we can get well-controlled 0.5ns steps between consecutive delay cells.

From the oscillator we also have to derive the pulse repetition clock for transmission. A programmable divider will provide for the flexibility to send pulses at the desired rates. The per-stage divider jitter is proportional to the output slope[15], and in a 0.13 $\mu$ m CMOS process, these edges are around 30ps. The actual per-stage jitter is expected to be less than that. With careful design, this jitter is not expected to be the dominant contribution.

### 7. DIGITAL BACKEND

The digital backend processing is rather large; implementing 128 programmable matched filters, 1,411 spreading-gain correlators with peak detection on their outputs, and control logic for acquisition and synchronization. Because the size of a fully parallel solution, searching all phases simultaneously over the entire pulse repetition period, is too large, some trade-offs need to be made with regard to the matched filter size and number of correlators.

The area trends versus matched filter coefficient bit-width and number of taps are shown in Figure 9. Increasing the tap size improves acquisition, but causes a geometric increase in area. Increasing bit-width linearly increases area with a tap-size dependent slope.

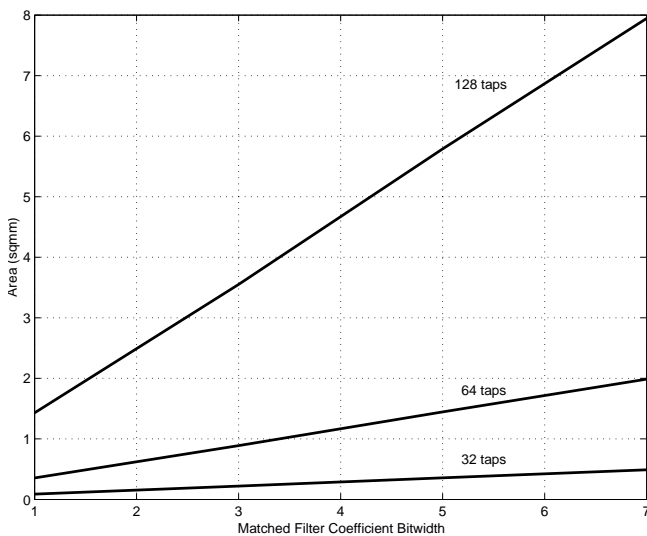


Figure 9. Matched Filter Area Considerations

There is also a geometric increase in complexity for correlating over the spreading sequence. Searching all 1024 phases simultaneously is prohibitively large. Figure 10

shows the trade-off between the total digital area (matched filter and correlator) and acquisition time versus the number of phases of the spreading-sequence are correlated in parallel. For our design, an area of approximately 10 mm<sup>2</sup> was available for the digital section, allowing for 11 phases searched in parallel.

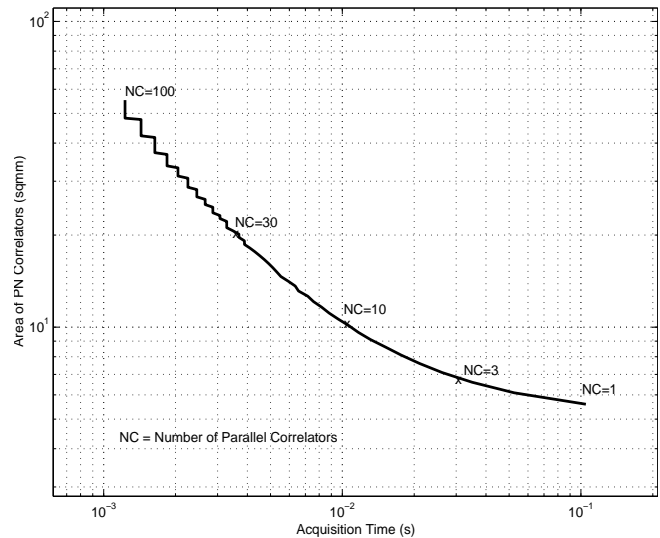


Figure 10. Total Area Vs. Acquisition

### 8. INTERFERENCE

Since the UWB interference caused to existing narrowband systems is of critical importance, a system requirement was imposed that the UWB radio would cause negligible degradation of sensitivity over the transmit bandwidth being used. For a single active UWB radio, we may constrain the power spectral density of the transmit power received to be equal to or less than the thermal noise floor over that bandwidth. To derive a conservative estimate for the transmit power constraint in the case of multiple UWB radios operating, we analyze the aggregate power received by a narrowband radio surrounded by an infinite 2-dimensional array of equal power UWB transmitters spaced at multiples of  $d$  meters, assuming a path loss coefficient of  $n$  for the indoor channel.

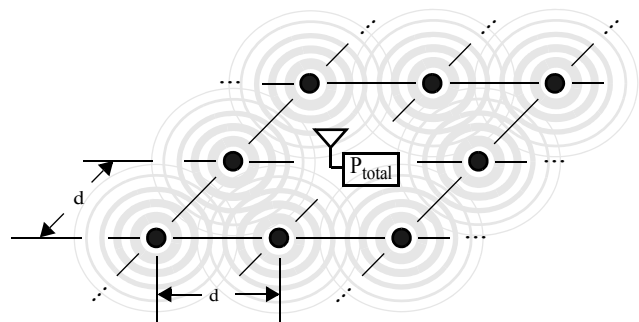


Figure 11. Interference from an Array of UWB Radios

Assuming the narrowband radio receives  $P_{1m}$  at 1 meter, approximately flat over frequency, from a single UWB transmitter, then aggregate power received,  $P_{total}$ , is:

$$P_{total} = P_{1m} \cdot \left( \sum_{x \neq 0} \sum_{y \neq 0} \frac{1}{(d\sqrt{x^2 + y^2})^n} \right)$$

Using a path loss coefficient of  $n=2.4$  [10], we find that for a spacing of  $d=1$  meter,  $P_{total}$  is equal to only  $12.6P_{1m}$ , and for a spacing of  $d=3$  meters,  $P_{total} = 0.9P_{1m}$ . By setting this total power to an acceptable level of interference, we may back-calculate the maximum allowable transmit power, to ensure negligible impact on existing narrowband channel users. While this analysis is rather approximate, not taking into account antenna directivity, etc., it illustrates that the aggregate interference caused by UWB may be relatively small, even for high densities.

## 9. CONCLUSION

The architecture of an integrated, low power, ultra-wide-band transceiver intended for low-rate, indoor wireless systems was presented. The implementation issues of this system, including clock generation, conversion bit-widths, gain, noise, and the choice of pulse rate versus pulse amplitude were discussed in relation to their impact on both performance and circuit design constraints. In addition, the issue of interference was discussed, and the implications for an “imperceptible” operating regime were explored.

## ACKNOWLEDGEMENTS

This research was supported by the Office of Naval Research (Award No. N00014-00-1-0223), a Multidisciplinary University Research Initiative (MURI) grant from the Department of Defense. (Grant #065861), and the industrial members of the Berkeley Wireless Research Center.

## REFERENCES

- [1] FCC, *First Report and Order*, FCC 02-48, Feb. 14, 2002.
- [2] R. A. Scholtz, “Multiple Access with Time-Hopping Impulse Modulation,” *Proceedings of MILCOM '93*, pp. 447-50, vol. 2, Oct. 11-14, 1993.
- [3] R. A. Fleming, C. E. Kushner, “Spread Spectrum Localizers,” U.S. Patent 5,748,891, May 5, 1998.
- [4] P. II. Withington, L. W. Fullerton, “An Impulse Radio Communications System,” *Proc. of the Intl. Conf. on Ultra-Wideband, Short-Pulse Electromagnetics*, pp. 113-20, Oct. 1992.
- [5] W. Namgoong, “A Channelized DSSS Ultra-Wideband Receiver,” *Proceedings RAWCON 2001*, pp. 105-8, Aug. 19-22 2001.
- [6] R. Hoctor, H. Tomlinson, “Delay-Hopped Transmitted Reference RF Communications,” *IEEE Conf. on Ultra-Wideband Systems and Technologies 2002*, May 20-21, 2002.
- [7] G. M. Maggio, N. Rulkov, L. Reggiani, “Pseudo-Chaotic Time Hopping for UWB Impulse Radio,” *IEEE Trans. Circuits and Systems-I*, pp. 1-12, Dec. 2001.
- [8] J.G. Proakis, *Digital Communications*, 3rd Edition, McGraw Hill, New York, 1995.
- [9] C. J. Le Martret, G. B. Giannakis, “All-Digital PAM Impulse Radio for Multiple-Access Through Frequency-Selective Multipath,” *Proceedings of GLOBECOM '00*, vol. 1, pp. 77-81.
- [10] D. Cassioli, M. Z. Win, A. F. Molisch, “The Ultra-Wide Bandwidth Indoor Channel: From Statistical Model to Simulations,” *IEEE J. Select Areas Comm.*, vol. 20, no. 6, p. 1247-57, Aug. 2002.
- [11] J. D. Taylor (Ed.), *Introduction to Ultra-Wideband RADAR Systems*, CRC Press, Boca Raton, FL, 1995.
- [12] J. A. Crawford, *Frequency Synthesizer Design Handbook*, Artech House, Norwood, MA, 1994.
- [13] H. Tang, Ph. D. Thesis, University of California at Berkeley, Expected Dec. 2002.
- [14] Q. Huang, P. Basedau, “A 200 $\mu$ A, 78MHz CMOS Crystal-Oscillator Digitally Trimmable to 0.3PPM,” *Int. Symp. on Low Power Elect. and Design*, pp. 305-8, 390. Aug., 1996.
- [15] T. C. Weigandt, B. Kim, P. R. Gray, “Analysis of Timing Jitter in CMOS Ring Oscillators,” *IEEE Int. Symp. Circuits and Systems*, vol. 4, p. 27-30, June 1994.
- [16] B. Kim, T. C. Weigandt, P. R. Gray, “PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design,” *IEEE Int. Symp. Circuits and Systems*, vol. 4, p. 31-4, June 1994.