A Fully Integrated Multi-Output CMOS Frequency Synthesizer For Channelized Receivers

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Abstract

A fully integrated frequency synthesizer that generates multiple frequencies for use in frequency channelized receivers is designed in 0.25µm CMOS technology. Many of the unique features of this receiver have been exploited to design a highly integrated and power efficient multi-output frequency synthesizer including the poly-phase filters. The synthesizer generates 4, 5, 6, and 7 GHz signals while dissipating 120mW.

I. Introduction

Although great headway has recently been made in efficient implementation of narrowband communication systems, very little work on the implementation of wideband communication radios exist by comparison. More recently, however, there have been a growing number of research institutions starting research in this area. Motivation for such research activities are based on, for example, the emergence of the ultra-wideband (UWB) radio and the need for multi-modal radios to support the myriad of existing communication standards.

Among the technical challenges in designing a wideband communication radio are in achieving wideband signal amplification and high-speed/high-resolution analog-to-digital conversion (ADC). A promising approach for overcoming these problems is to channelize the received wideband signal into multiple frequency bands using a bank of mixers and low-pass filters as shown in Figure 1. Multiple ADC's are then employed to operate at a fraction of the effective sampling frequency [1]. Such architecture relaxes the design of the LNA, the sample/hold circuitry and the dynamic range of each of the ADCs. Signal detection is performed in the digital domain based on the channelized samples.

Critical to the realization of such frequency channelized receiver is the availability of a fully integrated multi-output frequency synthesizer. This paper describes the design of such a synthesizer in 0.25µm CMOS technology for a frequency channelized UWB receiver. This design receives from 3.5 GHz to 7.5 GHz, which corresponds to a bandwidth of approximately 4 GHz.

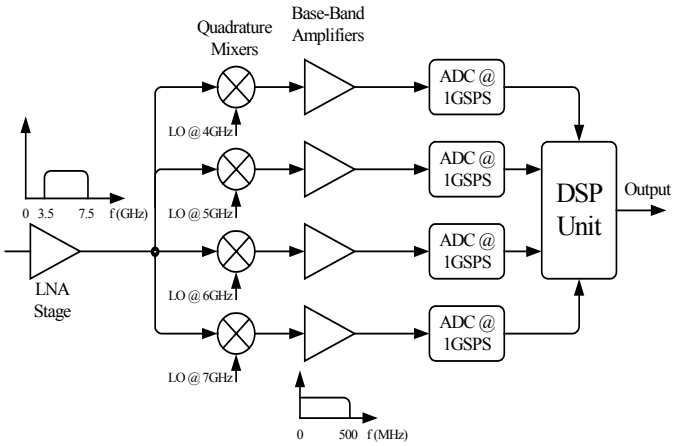

Fig. 1. Receiver architecture

The organization of this paper is as follows. Section II describes some of the synthesizer design challenges as well as different design approaches. In Section III, architecture of our frequency synthesizer is presented. Section IV describes the synthesizer building blocks and the reasons for choosing them. Section V discusses the phase noise issues in our synthesizer. The results of the simulation and conclusions are presented on Section VI and VII, respectively.

II. Frequency Synthesizer

Unlike narrowband systems that need one local oscillator, multiple frequencies have to be generated simultaneously in the channelized receiver. A straightforward approach for generating these frequencies is to parallelize multiple single-output frequency synthesizers, each of which is synchronized to the same reference clock. The drawback of such approach is the need for multiple digital frequency dividers, which is often the main power consuming block especially in a CMOS implementation. To reduce power, our synthesizer employs

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mixers and injection-locked frequency divider (ILFD) as described in the following section.

Another approach for generating simultaneous different frequencies is to use a non-linear device to generate all the harmonics and to select the desired tones using band-pass filters. Active band-pass filters, which generally dissipate large power, would be required because of the low quality factor on-chip inductors. This approach also suffers from poor spectral purity and high phase-noise.

III. Proposed Synthesizer Architecture

The proposed architecture is a multi-mixer stage PLL, which employs mixer stages instead of divider stages in the feedback loop. In this design, a 1GHz reference input signal is used to generate 4, 5, 6 and 7 GHz signals (Fig. 2). The 1GHz reference signal is selected because this corresponds to the ADC sampling frequency. As described in [1], the generated sinusoidal signals must be frequency locked to the sampling frequency to simplify the digital reconstruction process in the frequency channelized receiver.

To minimize power, a sequential approach has been used to generate the desired output frequencies. In the first stage, the 1GHz reference input has been used to generate a 4GHz output signal. The first stage loop consists of a VCO stage, an ILFD [2] that divides the frequency by two, two mixer stages that down-convert the ILFD output and an active loop filter. After the initial divide-by-two in the loop, two mixers are used to generate the phase error signal. The same result can be achieved by replacing the ILFD with another two mixer stages. However, the loop gain in this case would be significantly reduced, since passive mixers are used to minimize power.

In the subsequent stages, the output of the previous stage and the 1GHz input signal are used to mix the output of the VCO in the current stage as shown in Figure 2. Each stage then generates an output signal with a frequency that is 1GHz higher than the previous one.

The loop filter in each stage has been optimized to reduce the phase noise and the spurious tones. A set of poly-phase filters has also been added to each of the outputs to generate the in-phase and quadrature LO signals.

IV. Synthesizer Building Blocks

A. Voltage-Controlled Oscillator / Poly-Phase Filter

The proposed synthesizer uses cross-coupled CMOS VCO's with on-chip spiral inductors [3]. To minimize the phase noise, the on-chip spiral inductors are chosen to maximize the effective parallel impedance of the RLC tank at resonance [2]. Specifically, in the 4GHz VCO, a 3.5 turn

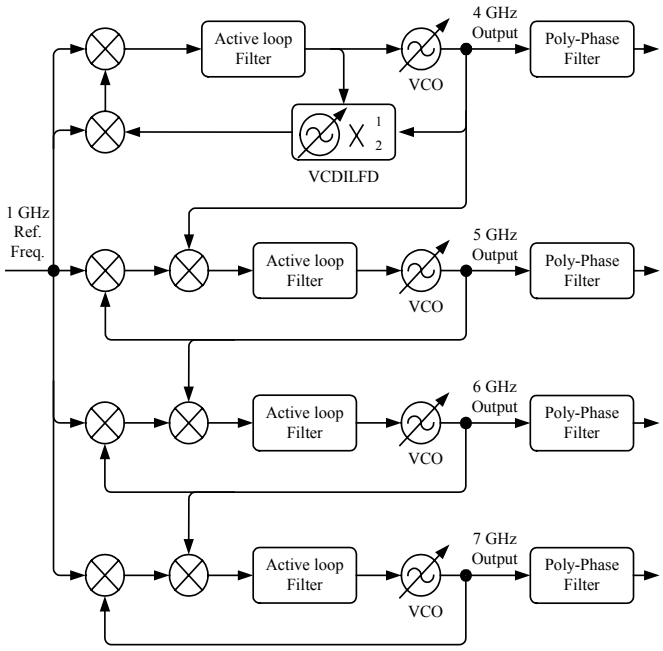

Fig. 2. Frequency synthesizer block diagram

spiral inductor has been used with an approximate Q of 7; in the 5GHz, 6GHz, and 7GHz VCO's, a 2.5 turn spiral inductor has been used with approximate Q's of 7, 7.3 and 7.5, respectively. The inductors are realized as a single spiral on the topmost metal layer (metal 5).

The varactors are realized as accumulation-mode MOS capacitors. All the varactors consist of the same size varactor fingers with different number of these fingers used for each of the VCO's. The fingers are 2.5 μm wide and 0.5 μm long. The number of fingers in 4, 5, 6 and 7 GHz VCO's is 7, 5, 5, and 4, respectively. The quality factor of these varactors at their operating frequencies is estimated to exceed 50.

The poly-phase filters are connected directly to the VCO without a buffer. Since the VCO output signal amplitude is large, the non-linearity in the active buffers could generate spurious tones. The removal of the buffers also reduces power consumption. The drawback of omitting the buffers is that the resistive part of the poly-phase filter contributes to the losses in the RLC tank. By careful design, however, the resistive loading effect caused by the poly-phase filter is made small (approximately 5 to 10 percent).

The poly-phase filters consist of two RC stages followed by a common-gate buffer stage. Since the amplitude at the input of this buffer is attenuated by the RC stages, the non-linearity in the buffer becomes less significant.

B. Mixers

Two back-to-back mixers are used to generate the error

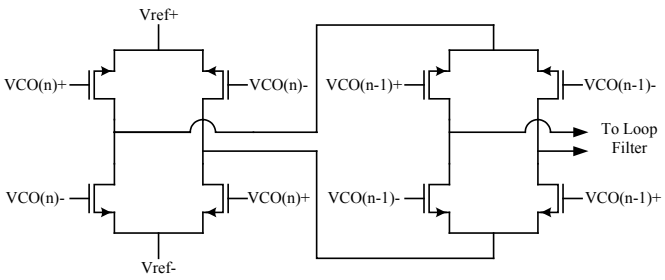

Fig. 3. Schematic of back-to-back mixers

signal. In the first stage, an ILFD is used in addition to the back-to-back mixers to first divide the 4GHz VCO output signal by two. Mixers are used to generate the error signal instead of the more commonly employed phase-frequency detector (PFD) because of the high signal frequencies. At these frequencies, the PFD is difficult to implement, dissipates significantly more power than the mixer, and increases the phase noise in the loop. The passive mixers are employed as shown in Figure 3.

Except for the first stage, where the same reference 1GHz sinusoid is employed in back-to-back mixers, the VCO output is mixed with the 1GHz sinusoid (V_{ref}) followed by the VCO output of the previous stage (Fig. 3). This mixing order reduces the potential for coupling between the two VCO outputs when transistor mismatches cause signals to leak. If the VCO outputs of the two consecutive stages were mixed, spurious tones close to the desired signal frequency could appear, which are not easily filtered out. Hence, the first mixing is with the reference 1GHz sinusoid to maximize the frequency difference between the mixing frequencies. In the second mixing, the coupling between the two mixing signals would not result in nearby spurious tones, since the output signal of the first mixer is at the same frequency as the VCO output of the previous stage.

C. Active Loop Filter

An active filter has been used with an amplification of approximately 20dB. The large amplification is needed to compensate for the loss in the back-to-back passive mixers. The bandwidth of the loop filter is chosen differently for each stage to minimize the spurious tones and the phase noise. In addition to the filtering operation, the active loop filter converts the differential error signal to a single-ended signal, which is necessary to drive the VCO's control voltage.

V. Phase Noise Issues

The phase noise in our synthesizer can be accurately modeled as being generated from three sources: the VCO's, the active low-pass filters, and the input reference signals

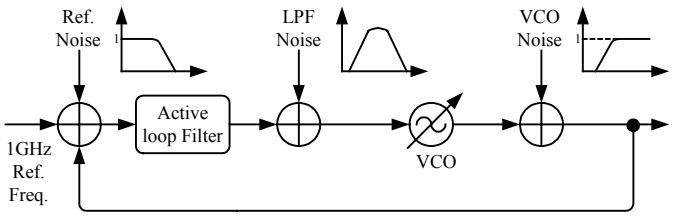

Fig. 4. Phase noise sources and their transfer functions to the output

(Fig. 4). We assume that the input phase noise provided externally is –120dBc/Hz at 1MHz [4]. Since this phase noise is small compared to that of the on-chip VCO, the loop filters are made wideband to filter out as much of the VCO phase-noise as possible [4]. The output phase-noise of each stage then becomes approximately the same as its input phase-noise. Wideband loop filters can be employed since the desired synthesizer frequencies are fixed. Also, the wideband loop filters help in the acquisition process in the presence of process and temperature variations. The loop bandwidth, however, cannot be made arbitrarily wide because of the spurious tones caused by the inter-modulation products. The loop bandwidth is set to be in the 100MHz range, which is approximately an order of magnitude smaller than the smallest inter-modulation frequency.

VI. Results Of Simulation

The entire synthesizer design has been simulated using SpectreRF. The phase noise values were obtained numerically based on extracted noise sources. Figure 5 shows the spectrum of the synthesizer outputs and Table 1 summarizes the performance numbers.

Table I
Synthesizer Performance

Reference Frequency f_{ref}	1GHz	1GHz	1GHz	1GHz
Synthesizer Output	4GHz	5GHz	6GHz	7GHz
Side-Bands (dBc)	-191	-189	-187	-186
Spur @ f_{ref} (dBc)	-78	-74	-77	-73
Spur @ 2 f_{ref} (dBc)	-28	-25	-29	-27
Phase-Noise @ 1 MHz (dBc/Hz)	-119	-119	-119	-119
Power Dissipation (mW)				
VCO	11.4	11.4	14.1	14.1
ILFD	5.6	N/A	N/A	N/A
Active Loop Filter	7.8	7.8	7.8	7.8
Poly-Phase Filter	5.1	9.2	9.2	9.2
Total	29.9	28.4	31.1	31.1
Supply Voltage	2.5V (VCO, ILFD, PPF)		89.3 mW	
	3.3V (Active Loop Filter)		31.2 mW	
Implementation (to be done)				
Estimated Die Area	2.5 mm^2			
Technology	TSMC 0.25 µm CMOS			

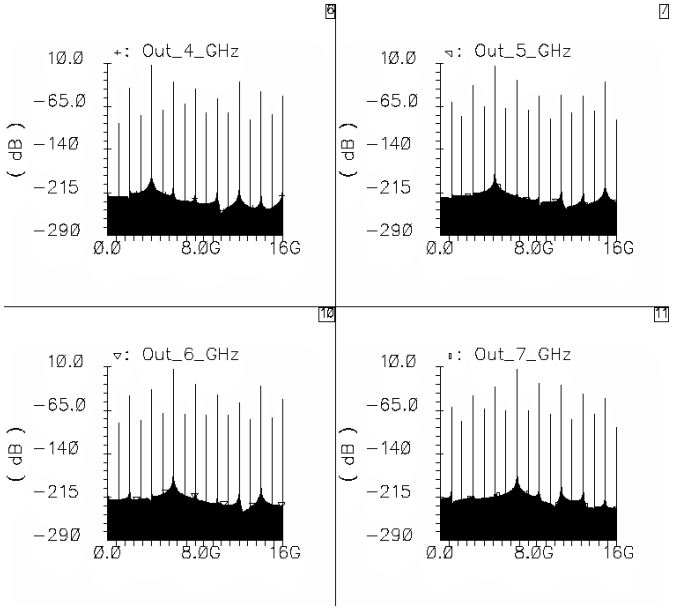

Fig. 5. Simulated output spectrum

VII. Conclusion

In this work, a fully integrated frequency synthesizer designed in 0.25µm TSMC CMOS process has been presented. This synthesizer has been designed for use in a frequency channelized UWB receiver. The goal in this design was to minimize the power consumption while achieving low phase noise characteristic and reasonable spectral purity. The layout area of the design is approximately 2.5 mm^2 and is dominated by the on-chip spiral inductors. Although a relatively large input reference signal of 1GHz is assumed, it can be easily replaced by an on-chip PLL that uses an off-chip crystal oscillator as a reference. Since the phase noises of the outputs of the synthesizer are dominated by the phase noise of their reference input, this design should be optimized for very low phase noise performance.

The multi-output synthesizer requirements of the frequency channelized receivers are very different from the conventional single-output synthesizers. Many of the unique features of the frequency channelized UWB receiver have been exploited to design a highly integrated and efficient synthesizer. Although comparing this design with a single-output frequency synthesizer may not be fair, Table 2 is added for comparison merely for the sake of completeness. This design is scheduled to be fabricated shortly with the rest of the frequency channelized UWB receiver.

Table II
Performance of Some Other Designs for Comparison

Reference	[2]	[7]
Reference Frequency	11 MHz	143 MHz
Synthesizer Output	4.84-4.994GHz	1.573GHz
Spur @ f_{ref} (dBc)	< -45	< -45
Spur @ 2 f_{ref} (dBc)	< -54	< -55
Phase Noise @ 1MHz (dBc/Hz)	-101	N / A
Power Dissipation	25mW	36mW
Technology	0.24µm	0.5µm

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