

position modulation (PPM) signals, and show that when the scaling of the number of channel paths is not too rapid, these signals achieve the capacity at the limit of infinite bandwidth. This work is motivated by a recent surge in interest in ultra wide band systems, where spreading signals are often desired.

Our result can be seen as a middle ground between two previous results: 1. FSK with duty cycle achieves AWGN capacity for any number of channel paths and 2. direct sequence spread spectrum signals with continuous transmission (no duty cycle) have zero capacity in the limit, if the number of channel paths increases with the bandwidth. Our results for spreading signals with duty cycle, show that these signals can achieve AWGN capacity in the limit of infinite bandwidth, if the scaling of the number of channel paths is suitable.

In the limit of infinite bandwidth, DSSS systems where the receiver knows the path delays achieve AWGN capacity if the number of channel path is sub-linear in the bandwidth. PPM system too can achieve AWGN capacity in the limit of infinite bandwidth, but this is possible for smaller number of channel paths. A PPM system with a receiver that knows the path delays achieves AWGN capacity if $\frac{L \log \log W}{\sqrt{\log W}} \rightarrow 0$ where L is the number of channel paths and W is the bandwidth, and has zero capacity if $\frac{L}{\log W} \rightarrow \infty$.

In systems that do not have any channel knowledge at the receiver, we show that DSSS systems can achieve AWGN capacity if $\frac{L}{W/\log W} \rightarrow 0$ as the bandwidth increases. PPM systems achieve AWGN capacity in single path channels, but it is unclear if they can achieve AWGN capacity if the channel has more than one path.

The effect of duty cycle can be understood in terms of the channel uncertainty a communication system faces. The data rate is penalized when the receiver has to estimate the channel, so seldom usage of the channel leads to small channel uncertainty and small penalty. Each transmission period should last as long as the channel does not change, to minimize the channel uncertainty penalty. The spectral efficiency of the modulation scheme plays an important role in determining the channel uncertainty a system handles. A system with low spectral efficiency can pack a small number of bits into each transmission period, and thus it is forced to transmit often. Thus, low spectral efficiency forces the communication system to estimate the channel often, and suffer from a large penalty on its data rate.

The difference between DSSS and PPM systems comes about because of their different spectral efficiencies. PPM is an orthogonal modulation, so the number of bits is can transmit per given time increases logarithmically with the bandwidth, where the number of bits a DSSS transmitter can send per given time increases linearly. Our results show that the spectral efficiency has a first order role in determining data rates in the limit of infinite bandwidth; the spectral efficiency of a modulation scheme determines *whether* this scheme can achieve AWGN capacity under given multipath conditions. This result is related to Verdú's [6], where the role of the spectral efficiency is second order. The channel model there is such that the channel uncertainty does not change as the limit is taken. The spectral efficiency determines in [6] *how fast* the AWGN capacity is approached in the limit of zero SNR, and in our work it determines *whether* the AWGN capacity is achieved at the limit.

After presenting the channel model and the signals in Section 2, we move directly to a discussion of the results in Section 4. Section 5 then presents bounds on the data rates of DSSS and PPM system where the receiver knows the channel path delays. Section 6 presents the penalty due to the path delays.

2 Channel Model and Signal Modulations

The natural model for an ultra wide band channel is real, because there is no obvious ‘carrier frequency’ that defines the phase of complex quantities. The channel is composed of \tilde{L} paths:

$$Y(t) = \sum_{l=1}^{\tilde{L}} A_l(t)X(t - d_l(t)) + Z(t)$$

The received signal $Y(t)$ is matched filtered and sampled at a rate $1/W$, where W is the bandwidth of the transmitted signal. Thus we get a discrete model of the channel. We assume a block fading model: the channel remains constant over coherence periods that last T_c , and changes independently between coherence periods. The paths delays are in the range $[0, T_d)$, where the delay spread T_d is assumed much smaller than the coherence period, so signal spillover from one coherence period to the next is negligible. Considering a double sided noise density $\frac{N_0}{2}$ the discretized and normalized channel is modeled by

$$Y_i = \sqrt{\frac{2PT_c}{\theta N_0 K_c}} \sum_{m=1}^{\tilde{L}} A_m X_{i-\tau_m} + Z_i \quad i = 0, \dots, \lfloor T_c W \rfloor - 1 \quad (1)$$

with $K_c = \lfloor T_c W \rfloor$. The noise $\{Z_i\}$ is real and Gaussian, and the normalization requires that the path gains $\{A_m\}$ and the transmitted signal $\{X_i\}$ are scaled so that $E(\sum A_m X_{i-m})^2 = 1$. If $\{A_m\}$ are independent and zero mean, the scaling requirement is $\sum E[A_m^2] = 1$ and $E[X_i^2] = 1$. This normalization ensures that $E[Z_i^2] = 1$. P is an average received power and θ is a duty cycle parameter that equals the fraction of time used for transmission.

In order to avoid complications at the edge of the coherence interval, we approximate the channel using a cyclic difference over K_c ($n \equiv n \bmod K_c$ instead of a simple difference. The difference is negligible if the delay spread is much smaller than the coherence time.

$$Y_i = \sqrt{\frac{2PT_c}{\theta N_0 K_c}} \sum_{m=1}^{\tilde{L}} A_m X_{(i-\tau_m)} + Z_i \quad i = 0, \dots, \lfloor T_c W \rfloor - 1 \quad (2)$$

We note that when X is a PPM signal from Section 2.2, the circular formulation (2) is identical to the original model (1).

The path delays $\{\tau_m\}$ are bunched into resolvable paths, separated by the system time resolution $\frac{1}{W}$. The number of resolvable paths L is defined by summing over the paths with similar delays:

$$G_l = \sum_{m: \frac{l}{W} \leq \tau_m < \frac{l+1}{W}} A_m \quad 0 \leq l < \lfloor T_d W \rfloor$$

The path delays $\{D_l\}_{l=1}^L$ are integers between 0 and $\lfloor WT_d \rfloor - 1$.

$$Y_i = \sqrt{\frac{\mathcal{E}}{K_c}} \sum_{l=1}^L G_l X_{i-D_l} + Z_i \quad i = 0, \dots, \lfloor T_c W \rfloor - 1$$

where $\mathcal{E} = \frac{2PT_c}{N_0 \theta}$. The channel gains are real, we assume that they are IID and independent of the delays. The delays are assumed IID uniform over $0, \dots, \lfloor WT_d \rfloor - 1$.

The systems we consider do not use channel information at the transmitter.

2.1 Direct Sequence Spread Spectrum Signals

Each symbol contains a random series of IID K_C Gaussian values $\{X_i\}_{i=0}^{K_C-1}$ with zero mean, and an energy constraint is satisfied:

$$E \left[\frac{1}{K_c} \sum_{i=0}^{K_c-1} X_i^2 \right] \leq 1 \quad (3)$$

We define the autocorrelation of the signal

$$C(m, n) \equiv \frac{1}{K_c} \sum_{i=0}^{K_c-1} X_{i-m} X_{i-n} \quad \forall m, n$$

The upper bound on DSSS capacity (Section 5.1) is valid also for another type of signal, where X is composed of pseudo-random sequences of K_C chips. The empirical autocorrelation of the input is bounded and the signal has a delta-like autocorrelation:

$$|C(m, n) - \delta(n, m)| \leq \frac{d}{WT_c} \quad (4)$$

where d does not depend on the bandwidth.

In either case (IID or pseudo-random chips) the duty cycle, with parameter $0 < \theta \leq 1$, is used over coherence times: of each period $\frac{T_c}{\theta}$, one period of T_c is used for transmission and in the rest of the time the transmitter is silent.

2.2 PPM Signals

Signaling is done over periods T_s long, with $\lfloor T_s W \rfloor$ positions in each symbol. A guard time of T_d is taken between the symbols, so the symbol period is $T_s + T_d$. The symbol time T_s is typically in the order of the delay spread or smaller. It does not play a significant role in the results. Each symbol is of the form:

$$X_i = \begin{cases} \sqrt{\frac{K_c(T_s+T_d)}{T_c}} & \text{one position of each group of } \lfloor T_s W \rfloor \text{ positions} \\ & \text{with } n \lfloor (T_s + T_d) W \rfloor \leq i \leq n \lfloor (T_s + T_d) W \rfloor + \lfloor T_s W \rfloor - 1 \\ & \text{High position selected IID uniform over } \lfloor T_s W \rfloor \text{ possibilities} \\ 0 & \text{other positions} \end{cases}$$

$$n = 0, 1, \dots, \left\lfloor \frac{T_c}{T_s + T_d} \right\rfloor - 1$$

$$i = 0, 1, \dots, \lfloor T_c W \rfloor - 1$$

The symbol timing is illustrated in Figure 1. The duty cycle parameter $0 < \theta \leq 1$ is used in Sections 5.3 and 5.4 over coherence times: of each period $\frac{T_c}{\theta}$, one period of T_c is used for transmission and in the rest of the time the transmitter is silent. Section 5.3 also calculates an upper bound on PPM data rates with a shorter transmission period.

3 Summary of the Results

Theorem 1 *DSSS systems with duty cycle, where the receiver knows the path delays, achieve $C_{\text{DSSS}} \rightarrow C_{\text{AWGN}}$ as $W \rightarrow \infty$ if $\frac{T_c}{W} \rightarrow 0$.*

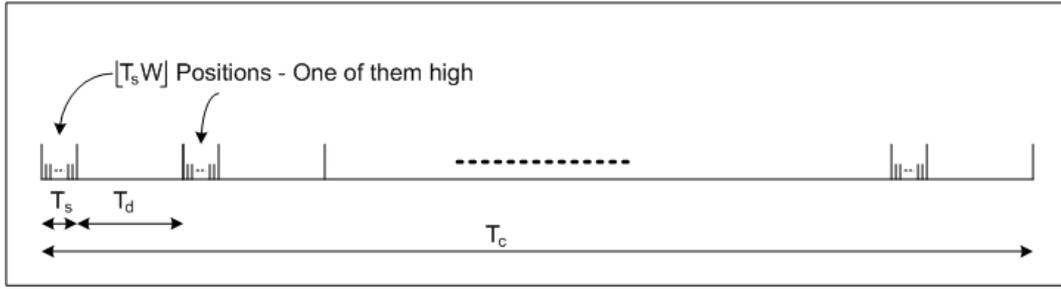


Figure 1: PPM symbol timing.

Theorem 2 *DSSS systems with duty cycle, where the receiver does not know the path delays or gains, achieve $C_{\text{DSSS}} \rightarrow C_{\text{AWGN}}$ as $W \rightarrow \infty$ if $\frac{L \log W}{W} \rightarrow 0$.*

Theorem 3 *DSSS systems with duty cycle, where the receiver does not know the path delays or gains, achieve $C_{\text{DSSS}} < C_{\text{AWGN}}$ in the limit $W \rightarrow \infty$ if $\frac{L}{W} \rightarrow \alpha$ and $\alpha > 0$.*

Theorem 4 *PPM systems with duty cycle, where the receiver knows the path delays, achieve $C_{\text{PPM}} \rightarrow C_{\text{AWGN}}$ as $W \rightarrow \infty$ if $\frac{L \log \log W}{\sqrt{\log W}} \rightarrow 0$.*

Theorem 5 *PPM systems with duty cycle, where the receiver does not know the path delays or gains, achieve $C_{\text{PPM}} \rightarrow C_{\text{AWGN}}$ as $W \rightarrow \infty$ if $L = 1$.*

Theorem 6 *PPM systems with duty cycle, where the receiver does not know the path delays or gains, achieve $C_{\text{PPM}} \rightarrow 0$ as $W \rightarrow \infty$ if $\frac{L}{\log W} \rightarrow \infty$.*

In the case of an infinite number of paths and receiver knowledge of the path delays, the fastest increase of the number of paths that a system can tolerate depends on its spectral efficiency.

A direct sequence spread spectrum system with receiver knowledge of the path delays, can tolerate a sub-linear increase of the number of paths with the bandwidth, and achieve AWGN capacity. We see this at the lower bound (8), that equals C_{AWGN} in this case. If the number of paths increases linearly with the bandwidth, the data rate is penalized, as seen in Section 5.1. Without knowledge of the path delays or gains, a DSSS system can achieve AWGN capacity if $\frac{L}{W/\log W} \rightarrow 0$, as see in (8).

PPM systems with knowledge of the path delays at the receiver can achieve AWGN capacity in the limit of infinite bandwidth if the number of paths L increases with the bandwidth W slowly enough, namely $\frac{L \log \log W}{\sqrt{\log W}} \rightarrow 0$ (Section 5.4). If the number of paths is too large ($\frac{L}{\log W} \rightarrow \infty$), the data rate converges to zero, as seen in Section 5.3. Without knowledge of the delays at the receiver, PPM systems can achieve the channel capacity if there is a single path ($L = 1$). We note that PPM signal are flash signals as defined in [6], but the theory there applies to channels of fixed dimensions (the matrix \mathbf{H} there). In our case, the channel dimension and the channel uncertainty increase with the bandwidth.

4 Discussion

This section presents bounds on the data rates of direct sequence spread spectrum and PPM systems for different channels, computed in Sections 5 and 6. The channel and system parameters were chosen to represent a realistic low SNR ultra wide band channel. For the figures with

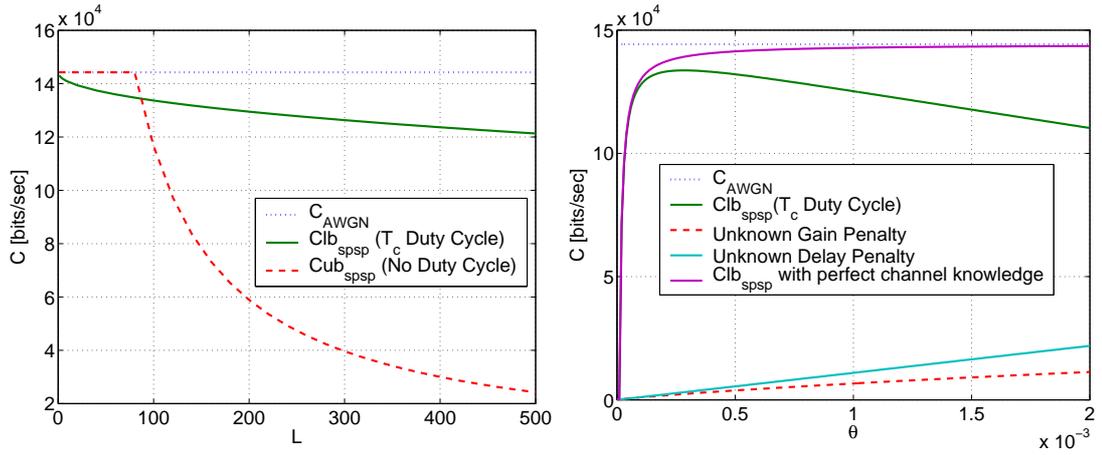


Figure 2: (Left Figure) DSSS capacity bounds, the receiver does not know the channel gains or delays. This plot contrasts an upper bound on DSSS data rate, when duty cycle is not used (bottom graph, from (6)) to a lower bound on the data rate when coherence period duty cycle is used (top graph, from (8)). C_{AWGN} is shown for reference.

Figure 3: (Right Figure) DSSS capacity lower bound vs. duty cycle parameter, the receiver does not know the channel path gains or delays. The middle curve shows the capacity lower bound (8), the dashed bottom curve shows the channel gain uncertainty penalty (the penalty in 7) and the one closely above it shows the delay penalty (12). The top curve shows the capacity of a system with perfect channel knowledge at the receiver. The capacity bound is the difference between the capacity with perfect channel knowledge and the channel uncertainty penalty. C_{AWGN} is shown for reference.

fixed bandwidth we use: Bandwidth $W=10$ GHz, $\frac{P}{N_0}=50$ dB (SNR=-50 dB at $W=10$ GHz), coherence period $T_c=0.1$ msec, delay spread $T_d=200$ nsec and PPM Symbol time $T_s=200$ nsec and $B^2d = 1$. For the figures with a fixed number of paths we use $L=100$.

4.1 The Advantage of Duty Cycle

Figure 2 shows the increase of data rate given by the usage of coherence period duty cycle, for DSSS systems. The figure compares the upper bound on DSSS capacity, where duty cycle is not used (bottom graph) to the lower bound on capacity when duty cycle is used. Both bounds decrease as the number of paths L increases because the channel uncertainty increases as L increases, and so does the penalty on the data rate.

4.2 The Duty Cycle Parameter

Figure 3 shows the lower bound on the data rate of a direct sequence spread spectrum system for different duty cycle parameter values. The bound is a difference between the data rate of a system with perfect channel knowledge at the receiver and the channel uncertainty penalty (gain penalty and delay penalty). The channel uncertainty penalty is small for low values of duty cycle parameter, because the channel is used less often as θ decreases. However, the data rate of a system with perfect channel knowledge is severely reduced if θ is too low. In this case, transmission occurs with high energy per symbol, where the direct sequence spread spectrum modulation is no longer spectrally efficient, so the data rate with perfect channel

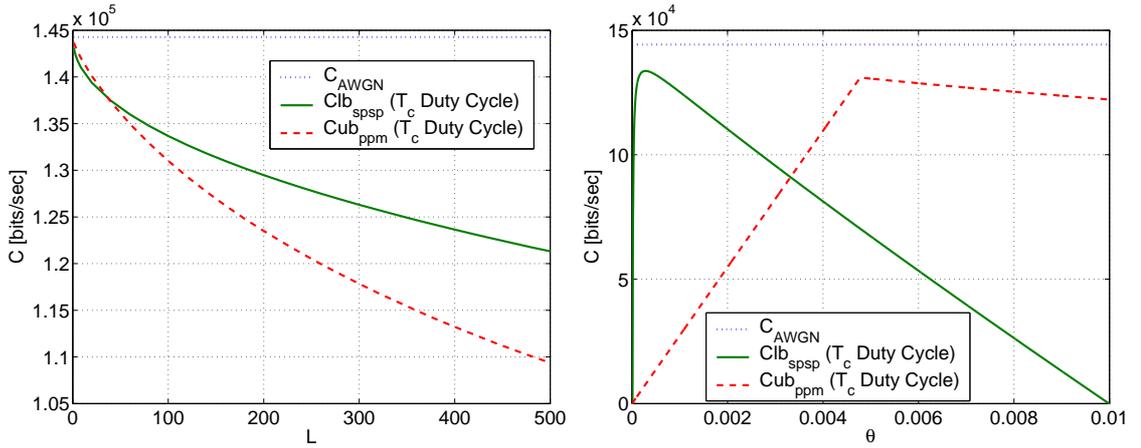


Figure 4: (Left Figure) DSSS and PPM capacity bounds. The DSSS lower bound (8) is calculated without channel knowledge at the receiver. The PPM upper bound (9) is calculated with a receiver that knows the channel delays but not the gains, coherence period duty cycle is used. C_{AWGN} is shown for reference.

Figure 5: (Right Figure) Capacity bounds vs. duty cycle parameter, the receiver knows the channel path delays but not the gains. DSSS capacity lower bound (8) is maximized at a lower duty cycle parameter than the PPM upper bound (9).

knowledge is reduced. Figure 3 shows that the duty cycle parameter must be chosen to balance the channel uncertainty penalty (that is large for large θ) and the spectral efficiency of the selected modulation, that increases with θ .

4.3 Spectral Efficiency

Figure 4 contrasts the achievable data rates of DSSS and PPM systems, when both use duty cycle on the coherence periods. Direct sequence spread spectrum achieves higher data rates because it has a higher spectral efficiency, thus it can pack more bits into each transmission period of length T_c . The number of bits per DSSS symbol depends linearly on the bandwidth, and the number of bits per PPM symbol depends logarithmically on the bandwidth, because PPM is an orthogonal modulation. The lower spectral efficiency of PPM forces it to transmit more often, and use a higher duty cycle parameter than DSSS (Figure 5). As a result, PPM systems suffer a higher channel uncertainty penalty than DSSS systems.

5 Data Rate Bounds

5.1 Upper Bound on DSSS Capacity

This bound is calculated for the case where the receiver knows the paths delays:

$$I(X; Y|D) \text{ [b/s]} \leq \max_{0 \leq \theta \leq 1} \min \left\{ W\theta \log_2 \left(1 + \frac{P}{N_0 W \theta} \right) \right\},$$

$$\left. \underbrace{\frac{8P^2T_c}{N_0^2\theta L} \log_2 e + \frac{4PT_d}{N_0T_c} B^2 d \log_2 e}_{(5)} \right\} \quad (6)$$

B is an upper bounds the paths gains: $|G_l| \leq \frac{B}{\sqrt{L}}$, this is a technical condition that follows [5]. d is defined in (4) for pseudo-random chips, and for IID chips it equals one.

The first part of (6) is the capacity of an AWGN channel used with duty cycle θ . It upper bounds the data rate for systems with channel knowledge at the receiver. In order to achieve the capacity at the limit of infinite bandwidth, the duty cycle parameter must be chosen so that $\theta W \rightarrow \infty$.

In the case of a linear increase in the number of paths with the bandwidth, the bound is significantly lower than the AWGN capacity in situations where $T_d \ll T_c$.

If the number of paths is sub-linear in W , the duty cycle can be chosen so that $\theta W \rightarrow \infty$ and $\theta L \rightarrow 0$ and the bounds in (5) become irrelevant. In this case the upper bound converges to C_{AWGN} in the limit of infinite bandwidth.

5.2 Lower Bound on DSSS Capacity

This bound is very similar to Theorem 3 in [5], it holds where the receiver knows the path delays.

$$I(X; Y|D) \text{ [b/s]} \geq C_{\text{AWGN}} - \min_{0 < \theta \leq 1} \left\{ \frac{\theta L}{T_c} \log_2 \left(1 + \frac{P}{N_0} \frac{T_c}{\theta L} \right) + \frac{3P^2}{2N_0^2\theta W} \log_2 e \right\} \quad (7)$$

With no channel knowledge at the receiver (path delay and gains unknown), we use (12):

$$I(X; Y) \text{ [b/s]} \geq C_{\text{AWGN}} - \min_{0 < \theta \leq 1} \left\{ \frac{\theta L}{T_c} \log_2 \left(1 + \frac{P}{N_0} \frac{T_c}{\theta L} \right) + \frac{3P^2}{2N_0^2\theta W} \log_2 e + \frac{\theta L}{T_c} \log_2 (W T_d) \right\} \quad (8)$$

At the limit of infinite bandwidth the data rate equals the AWGN capacity if $\theta W \rightarrow \infty$, $\theta L \rightarrow 0$ and $\theta L \log W \rightarrow 0$. The second condition may be dropped, as the third is stronger. These conditions can be met simultaneously if $L \log W$ is sub-linear in W , that is if $\frac{L \log W}{W} \rightarrow 0$.

5.3 Upper Bound on PPM Capacity

This bound holds for channels with IID Gaussian gains $G_l \sim N\left(0, \frac{1}{L}\right)$. The receiver knows the paths delays.

$$I(X; Y|D) \text{ [b/s]} \leq \max_{0 < \theta \leq 1} \min \left\{ \frac{\theta \log_2 T_s W}{T_s + T_d}, \frac{\theta W}{2} \log_2 \left(1 + \frac{2P}{\theta N_0 W} \right) - \frac{\theta L}{2T_c} \log_2 \left(1 + \frac{2PT_c}{\theta N_0 L} \right) \right\} \quad (9)$$

The first part of (9) is the PPM data rate.

5.4 PPM Lower Bound in the Infinite Bandwidth Limit

This bound is calculated using the probability of error of a specific receiver. As the bandwidth increases to infinity, the probability of error converges to zero. The receiver knows the path delays but not their gains.

The transmitter uses duty cycle over the coherence times, with $\theta \leq 1$ and a repetition code with $Q_r = \frac{2 \ln M}{\rho}$ symbols, $\rho = \frac{2P(T_s + T_d)}{\theta N_0}$, in order to average over the channel variation, the repetitions take place over different coherence times so they have independent channel realizations. The repetition code is set so that the transmitted (uncoded) data rate equals C_{AWGN} . The receiver averages its output over the Q_r symbols (as in *Telatar and Tse* [5], Section II). The receiver uses a threshold parameter $A = (1 - \epsilon)\rho + L$ for deciding on the transmitted value where $0 < \epsilon < \frac{1}{L}$. The bound holds for channels with IID Gaussian gains $G_l \sim N\left(0, \frac{1}{L}\right)$.

The Receiver Structure

For every symbol, the receiver calculates

$$s_i = \sum_{j=1}^L Y_{i+D_{j-1}}^2 \quad i = 1, \dots, M$$

Assuming that x_1 was transmitted the desired output is

$$s_1|x_1 \sim \chi^2\left(\frac{\rho}{L} + 1, L\right)$$

There are up to $L^2 - L$ overlap terms, that contain part of the signal

$$s_{\text{overlap}}(q) \sim \chi^2\left(\frac{\rho}{L} + 1, L - U_q\right) + \chi^2(1, U_q) \quad q = 1, \dots, Q_r$$

where U_q is the number of noise samples and $L - U_q$ is the number of signal samples, $1 \leq U_q \leq L - 1$. The summation here means that v_{overlap} is the sum of two independent random variables.

In addition, there are up to $M - 1$ noise terms:

$$s_{\text{noise}} \sim \chi^2(1, L)$$

The receiver averages over Q_r repetitions of the symbol:

$$v_i = \frac{1}{Q_r} \sum_{q=1}^{Q_r} v_i(q)$$

There are three types of error events, and the error probability is upper bounded using the union bound:

$$P(\text{error}) \leq P(v_1 \leq A) + Q_r(L^2 - L)P(v_{\text{overlap}} \geq A) + (M - 1)P(v_{\text{noise}} \geq A) \quad (10)$$

The first two probabilities are bounded using the Chebyshev inequality, and the third using the Chernoff bound. The probability of error converges to zero as $W \rightarrow \infty$ if

- $\epsilon^2 \theta L \log W \rightarrow \infty$ (first error event)
- $\frac{\theta \log W}{L \log(\theta \log W)} \rightarrow \infty$ and $\epsilon L \ll 1$ (second error event)
- $\theta L \rightarrow 0$ and $\epsilon \rightarrow 0$ (third error event)

The conditions on ϵ are easy to satisfy since it has a simple relation with the other parameters. If $\frac{L \log \log W}{\sqrt{\log W}} \rightarrow 0$ then all the conditions can be realized simultaneously.

Special Case: A Single Path

The special case of $L = 1$ is interesting, because the second error event does not exist there. The requirements for zero probability of error at the infinite bandwidth limit are $\epsilon^2 \theta \log W \rightarrow \infty$ (first error event), $\theta \rightarrow 0$ (third error event) and $\epsilon \rightarrow 0$ (third error event). These are simultaneously possible with a careful choice of θ and ϵ .

6 Path Delay Uncertainty Penalty

The path delays D are uniform over $(0, T_d]$. They are IID given that they have L different values.

$$\begin{aligned} I(Y; X) &= I(Y; X, D) - I(Y; D|X) \geq I(Y; X|D) - H(D) = I(Y; X|D) - \log \left(\frac{WT_d}{L} \right) \\ &\geq I(Y; X|D) - L \log(WT_d) \end{aligned} \quad (11)$$

This inequality is tight only if $L \ll WT_d$.

The penalty for unknown delays, in [bits/sec], with a duty cycle parameter θ and duty cycle period T_c :

$$-\frac{\theta H(D)}{T_c} \text{ [b/s]} \geq -\frac{\theta L}{T_c} \log_2(WT_d) \quad (12)$$

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