18.5 A 0.25μm CMOS 3b 12.5GS/s Frequency Channelized Receiver for Serial-Links

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As the speed of CMOS serial-links continues to improve, the achievable data bandwidth is limited by the off-chip environment such as wire losses in backplane traces and package parasitics. In such environments, well-known digital communication techniques such as coding, equalization, and multi-level signaling need to be employed to continue the increase of the serial-link data rates. Although increased digital processing capabilities allow the use of these techniques, the lack of available multi-bit ADCs has primarily limited their use. To achieve multi-bit data conversion at the signal Nyquist rate, a receiver architecture that decomposes the received wideband signal into multiple frequency subbands before digitizing at a much reduced frequency is designed and fabricated in 0.25μm CMOS process. This frequency-channelized receiver samples at an effective sampling frequency of 12.5GS/s with 3b resolution and requires no initial ADC offset compensation. The chip occupies 4.0mm^2 while consuming 1W at 2.5V supply. The functionality of the proposed receiver is demonstrated by correctly operating at 10Gsymbols/s in a channel with significant ISI.

Existing multi-bit receiver architectures operate by time-interleaving parallel ADCs with each operating at a fraction of the symbol frequency [1]. A fundamental problem of such parallel architecture is the mismatches among the demultiplexing channels, which are especially pronounced when operating at high data rates, as small transistors with corresponding small input capacitance are employed to meet the bandwidth requirements. Another drawback is the high sensitivity to sampling jitter caused by the large amounts of aliasing of the wideband input signal.

Instead of channelizing by time-interleaving ADCs, the received signal can be channelized into multiple frequency subbands with an ADC in each subband channel operating at a fraction of the effective sampling frequency [2]. An important advantage of channelizing in the frequency domain, instead of in the time domain, is that the digitized signal becomes less sensitive to channel mismatches and sampling jitter. Intuitively, this robustness results because the narrower signal bandwidth in each subband channel reduces the amount of aliasing caused by channel mismatches and sampling jitter. Another important advantage is that it obviates the need to generate accurately spaced clocks, which may become problematic as technology scales.

The proposed frequency-channelized receiver is shown in Fig. 18.5.1(a). The received signal is channelized into three subbands by employing two quadrature mixers and low-pass filters. Figure 18.5.1(b) shows the relationship between the signal bandwidth and the local oscillator frequencies. To further relax the ADC sampling requirements, the channelized subbands are sampled by time-interleaving two 3b ADCs, each operating at 1.25GS/s. A total of 10 ADCs are employed to achieve an effective sampling frequency of 12.5GS/s.

In the second and third subband channels, quadrature mixing is achieved by using a passive PMOS double-balanced topology (see Fig. 18.5.2) to achieve good linearity and to satisfy the bias requirements of differential CML. Unlike the sampler in the time-interleaved receiver, the mixer bandwidth needs to be only slightly wider than the subsequent lowpass filter bandwidth, which is approximately one-fifth of the signal bandwidth (see Fig. 18.5.1(b)). The signal attenuation caused by the mixer, whose magnitude is inversely proportional to the mixer bandwidth, can be readily compensated by amplifying in the subsequent stage, since the signal bandwidth is now much reduced.

The LPF stage provides the filtering operation and the variable gain amplification (VGA), so that the full dynamic range of the ADC is used. Since the signal bandwidth is approximately 1GHz after filtering, the decoupling of the filtering operation and the VGA becomes difficult. As a result, the amplifiers must vary the gain while keeping the lowpass filter bandwidth approximately constant. To achieve this, four stages of shunt-shunt feedback amplifiers are cascaded as shown in Fig. 18.5.3(a). The gain in each stage is –Rf/Rse, where Rf is the feedback resistance and Rse is the effective output impedance of the previous amplifier. Variable gain is achieved by adjusting the g_m of each amplifier using the gate voltage Vc (see Fig. 18.5.3(a)). The increase in g_m, for example, increases the loop gain, which causes the Rse to decrease proportionately. Since the effective input capacitance (Cie) of the next stage increases by the same amount, the bandwidth remains approximately constant. Experimental results of the LPF stage are shown in Fig.18.5.3(b). A variable gain of 10dB is achieved while the bandwidth remains approximately constant at 1GHz.

The channelized subband signals are each sampled by two time-interleaved ADCs, each operating at 1.25GS/s. The ADCs are a 3b flash-type ADC with un-balanced comparators followed by regenerative amplifiers and latches [3].

Figure 18.5.4 shows the generation of the local oscillator frequencies (fo and 2fo) when external fo of 2GHz is provided. Since designing a phase detector to operate at 2GHz is difficult, the 2nd-order PLL-based frequency doubler uses passive mixers for the phase detector. To achieve wide tracking range, another passive mixer is used as a frequency divider. The frequency doubler is found experimentally to achieve a tracking range of 450MHz and peak-to-peak jitter of 29.4ps at 4GHz.

The functionality of the channelized receiver is verified by digitizing binary data transmitted from a 10Gsymbol/s transmitter through 15cm of PCB trace and a 1m-long cable. To simplify the digital detection process and to achieve better ISI removing capability, cyclic prefix (i.e., append the last several symbols of the block to the beginning) is added to the transmitted signal. Single-carrier cyclic prefix systems enable frequency-domain equalization, which is shown to achieve higher performance at lower complexity compared to linear-type equalizers [4]. The ADC outputs from each subband channel are acquired and processed off-line using a PC to evaluate the performance. Figure 18.5.6(a) shows the measured eye diagram at the input of the receiver, which is completely closed. After sampling and processing off-line, the input to the slicer for 18,000 transmitted symbols is shown in Fig. 18.5.6(b). Two distinct regions corresponding to +1 and –1 are observed.

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References:
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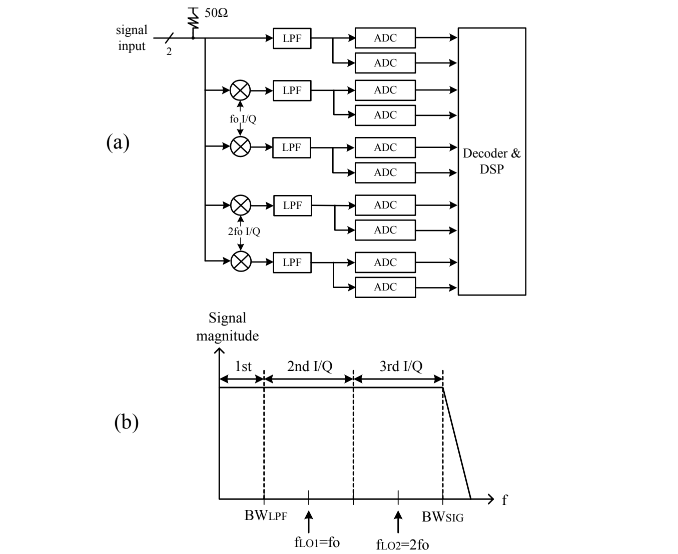

Figure 18.5.1: (a) Receiver architecture. (b) Frequency relationship.

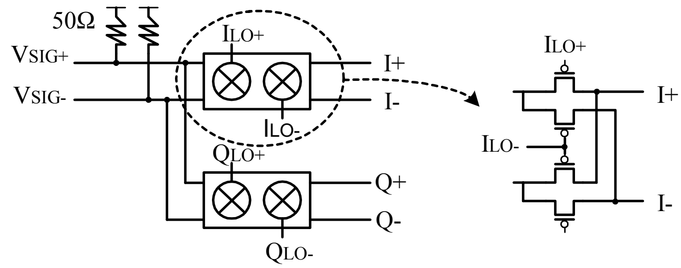

Figure 18.5.2: Quad-phase mixer.

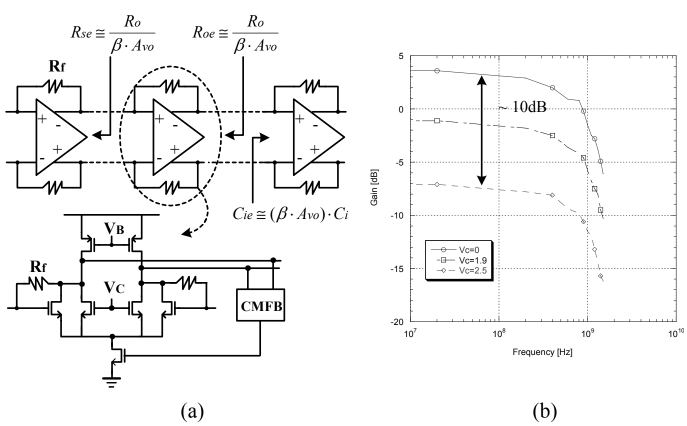

Figure 18.5.3: (a) 4-stage feedback LPF. (b) Gain response.

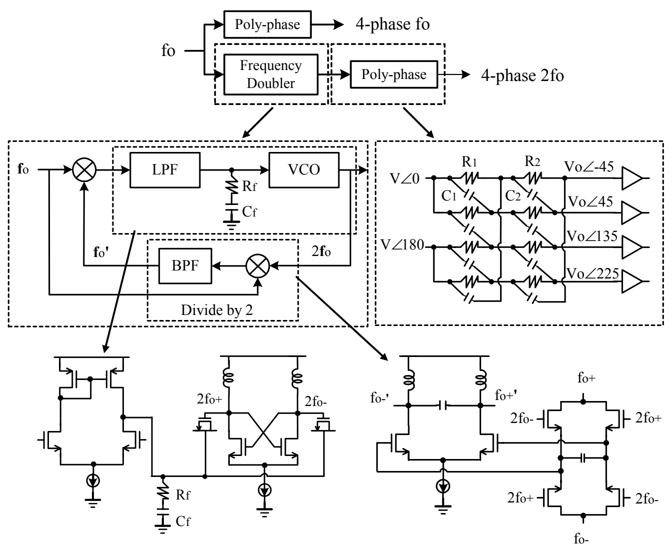

Figure 18.5.4: Frequency generation.

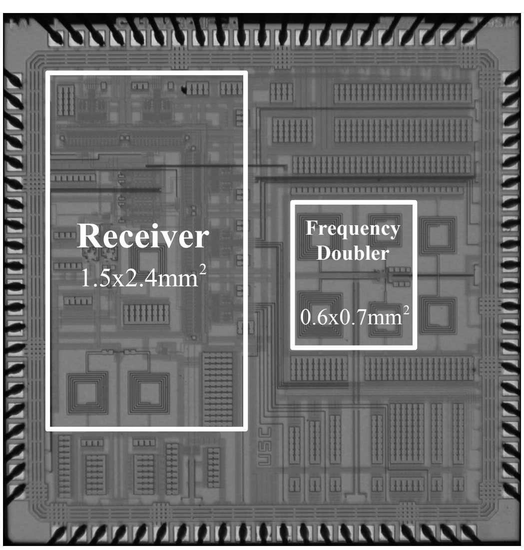

Figure 18.5.5: Chip micrograph.

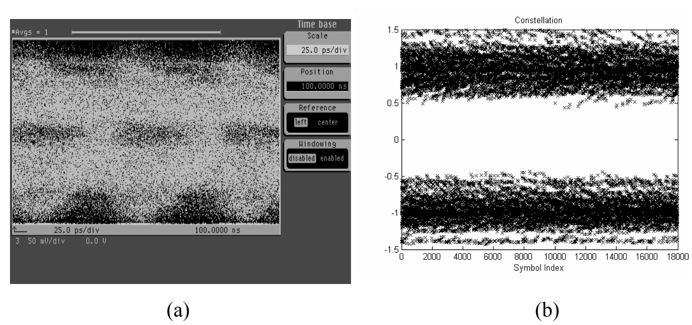

Figure 18.5.6: (a) Eye diagram at receiver input. (b) Slicer input after equalization.

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