A Sub-mW 960-MHz Ultra-Wideband CMOS LNA

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***Abstract*— This paper presents a sub-mW ultra-wideband (UWB) fully-differential CMOS low-noise amplifier (LNA) operating below $960\mathrm{MHz}$ for sensor network applications. By utilizing both NMOS and PMOS transistors to boost the transconductance, coupling the input signals to the back-gates of the transistors, and combining the common-gate and shunt-feedback topologies, the LNA achieves $13\,\mathrm{dB}$ of power gain, a $3.6\ \mathrm{dB}$ noise figure, $-15\ \mathrm{dB}$ input match, and $-10\ \mathrm{dBm}$ of $IIP3$ with only $0.72\,\mathrm{mW}$ of power consumption from a $1.2\mathrm{V}$ supply.**

I. Introduction

Ultra-wideband (UWB) technology enables two extremes of the wireless communication systems: one is the short-range, high data-rate applications such as the IEEE 802.15.3a standard operating at $3.1 - 10.6\mathrm{GHz}$; the other is the long-range, low data rate applications with accurate positioning capability, e.g. wireless sensor networks operating at below $960\mathrm{MHz}$. In both cases, low cost, low power solutions are needed to allow a high level of deployment.

CMOS technology is a promising candidate for UWB systems not only because the digital circuitry benefits from Moore's law, but scaling of the CMOS devices with increasing f_T and f_{max} also facilitates the processing of large bandwidth analog signals with low power. Therefore, it is expected that single chip UWB solutions will appear in the near future.

This paper focuses on the implementation of the LNA for UWB systems below $960\mathrm{MHz}$. According to FCC regulations, the Effective Isotropic Radiation Power (EIRP) for UWB operation is $-41.3\,\mathrm{dBm/MHz}$, which translates to less than $72\mu\mathrm{W}$ of radiation power if the whole $0-960\mathrm{MHz}$ bandwidth is utilized. This means that the system power consumption is no longer dominated by the radiation power, but rather by the power consumed in the circuitry itself. Thus, to enhance the efficiency of the transceiver and increase the battery life, circuit building blocks with extremely low power, say $1\mathrm{mW}$, are necessary.

For the $< 960\mathrm{MHz}$ UWB systems, since the operating frequency overlaps many other systems, e.g. the UHF TV band and cellular bands, the receiver must tolerate a large amount of in-band interference in addition to the ambient thermal noise. The input-referred receiver noise is given by

$$N_{RX} = N_{INTERFERE} + F \cdot N_{THERMAL} \tag{1}$$

where $N_{INTERFERE}$ is the interference noise, $N_{THERMAL}$ is the ambient thermal noise, and F is the noise figure of the receiver. In practice, the in-band interference can be so large that it dominates the receiver noise, i.e. $N_{INTERFERE} \gg N_{THERMAL}$, and the circuit noise figure can be relaxed without degrading the system performance. Thus the task of designing a UWB LNA for $< 960\mathrm{MHz}$ applications is no longer about pushing the noise figure to the fundamental limit [1][2], but rather to minimize the power consumption while achieving a moderate noise figure. From system consideration, LNA noise figure below 6dB is reasonable [3].

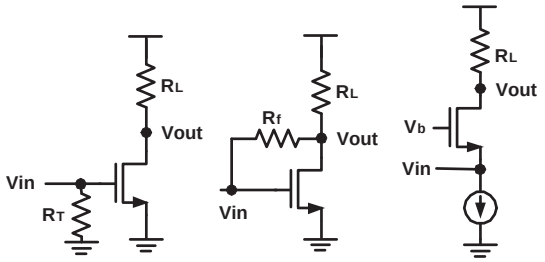

Fig. 1. Traditional wideband amplifiers: (a) Resistor-terminated common-source amplifier; (b) shunt-feedback amplifier and (c) common-gate amplifier.

II. Review of Traditional Wideband Amplifiers

The most popular amplifiers that can achieve power/voltage gain and 50Ω input impedance over a wide bandwidth are the resistor-terminated common-source amplifier, shunt-feedback (SFB) amplifier and common-gate (CG) amplifier (Fig. 1). Almost all the published wideband LNAs are based on either of these configurations [1][4][5][6]. Although the resistor-terminated common-source amplifier can achieve the lowest possible power while still providing 50Ω input impedance, the resistor R_T attenuates the signal and contributes thermal noise by itself and makes the noise figure easily go beyond $6\,\mathrm{dB}$, which is not tolerable. For both the SFB amplifier and CG amplifiers, the noise figure (ignoring noise contributed by R_f and R_L) is

$$F \geq 1 + \frac{\gamma}{\alpha}\frac{1}{g_m R_S} \tag{2}$$

where R_S is the input source resistance, γ is about $2/3$ for long-channel devices, and $\alpha = g_m/g_{d0}$ [7]. The input impedance of the shunt-feedback amplifier (ignoring capacitances) is

$$Z_{in,\text{Shunt-FB}} = \frac{R_f + R_L||r_o}{1 + g_m(R_L||r_o)} \geq \frac{1}{g_m} \tag{3}$$

and that of the common-gate amplifier is

$$Z_{in,\text{CG}} = \frac{r_o + R_L}{g_m r_o} \geq \frac{1}{g_m} \tag{4}$$

For both cases, the g_m has to be at least $20\mathrm{mA/V}$ in order to provide 50Ω of Z_{in}, and the corresponding noise figure is at least $1+\gamma/\alpha \sim 3\,\mathrm{dB}$. Assuming the current efficiency g_m/I_D

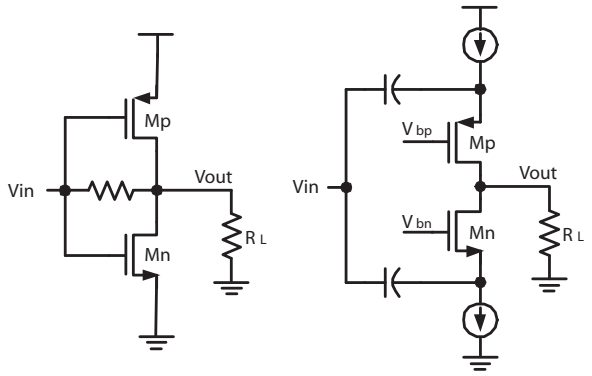

Fig. 2. Applying current-reuse technique to (a) shunt-feedback amplifier and (b) common-gate amplifier.

is $20\,\mathrm{V}^{-1}$, power consumption for each of the amplifiers will exceed $1\mathrm{mW}$ at $V_{DD} = 1.2\mathrm{V}$. Furthermore, because the LNA shares the substrate with baseband digital circuits in most of the UWB systems, a differential scheme is preferred to eliminate the on-chip switching noise. When an input voltage drives a differential pair, the voltage across each branch is halved, which leads to halving of the input current and doubling of the input impedance. To achieve a differential input match requires $Z_{in} = 25\Omega$, which in turn requires at least $4\mathrm{mW}$ of power consumption, and the noise figure stays above $1 + \gamma/\alpha$. It is thus concluded that for SFB and CG LNAs, when the targeting NF is above $\sim 3\,\mathrm{dB}$, the power consumption is set by the 50Ω input impedance.

III. LNA Circuit Design

A. Current Reuse Technique

To lower the power consumption, one can reuse the current by stacking the NMOS and PMOS transistors and having both act as amplifying devices [8]. As shown in Fig. 2, a PMOS device is stacked on top of the NMOS which enhances the transconductance. This increases the equivalent G_m from g_{mn} to $g_{mn} + g_{mp}$ and allows one to halve the current for the same input impedance and noise figure. It introduces more capacitance that decreases the bandwidth, a small penalty in advanced CMOS technologies.

B. Shunt-Feedback/Common-Gate Hybrid Topology

The two branches of a differential SFB or CG LNA act like two resistors in series to the input. This not only doubles the input impedance, but also attenuates the gate-source voltage across each transistor which degrades the gain and noise figure. If the input voltage can be applied to both transistors without division, the performance will be enhanced.

Fig. 3 shows the shunt-feedback/common-gate hybrid (SFBCG) topology. The input voltage is directly coupled to the gate and source terminals in each branch of the differential pair, but with opposite polarities. The positive input V_{in}^{+} is coupled to the gate nodes of M_{N1} and M_{P1}, which act as a SFB amplifier; it is also coupled to the source nodes of M_{N2} and M_{P2}, which is a CG amplifier. The transistors play

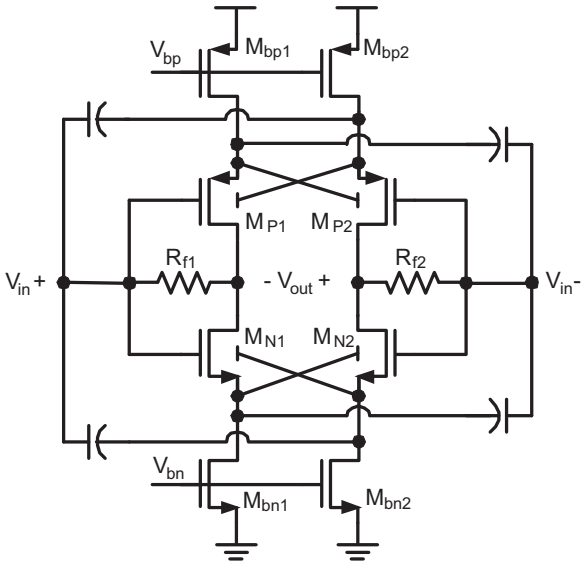

Fig. 3. The Shunt-Feedback/Common-Gate Hybrid (SFBCG) amplifier.

opposite roles for the negative input V_{in}^{-}. By combining these two topologies in a differential scheme, the input current is the sum of I_1 and I_2 and the input impedance becomes

$$Y_{in} = \frac{1 + 0.5(g_{m1} + g_{m2})R_L}{R_f + R_L} + \frac{0.5(g_{m1} + g_{m2})r_0}{r_0 + R_L||R_f} \tag{5}$$

$$Z_{in} \approx \frac{1}{g_{m1} + g_{m2}} = \frac{1}{2g_m} \tag{6}$$

which is four times smaller than that of a differential SFB or CG amplifier. Correspondingly, a factor of four reduction in power consumption is achieved for the same input impedance.

The noise figure of the SFBCG amplifier (assuming R_f and R_L are large) is

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{(g_{m1} + g_{m2})R_S} = 1 + \frac{\gamma}{\alpha}\frac{1}{2g_m R_S} \tag{7}$$

When input is matched ($R_S = 1/2g_m$), the noise figure $F = 1 + \gamma/\alpha$, which is the same as that of a differential SFB or CG amplifier, but with four times less power. This is due to the fact that the input voltage is now fully applied to the gate-source terminals without attenuation. The voltage gain of the SFBCG amplifier is the summation of the gains of a SFB and a CG amplifier

$$A_v = 1 + (g_{m1} + g_{m2})R_f \tag{8}$$

The current sources (M_{bn1}, M_{bn2}, M_{bp1}, and M_{bp2} in Fig. 3) provide high impedance and can be implemented by either transistors or RF chokes. The latter can save some voltage headroom which in turn allows a lower supply voltage and lower power consumption, but for operation below $1\,\mathrm{GHz}$, the inductance is too big to be implemented on chip.

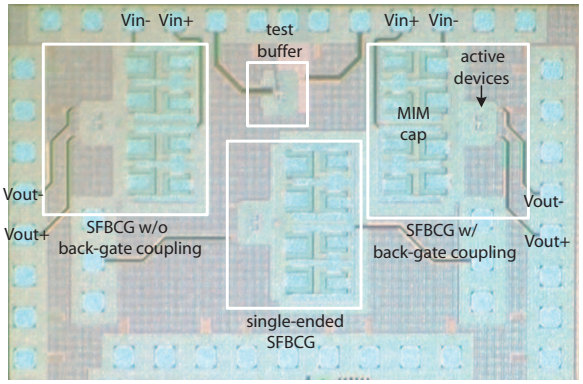

Fig. 4. Die photo of the SFBCG test chip.

C. Back-Gate Coupling in Triple-Well Process

In a triple-well process, one is allowed to connect the body terminals of devices to their source nodes. This eliminates the body effect and decreases the threshold voltage, which is beneficial to low-voltage analog circuits. In the SFBCG amplifier, since the two branches are balanced and have the same bias voltages, one can even cross-connect the bodies to the source nodes of the devices on the other side. Small-signal-wise, the bodies are shorted to their gates, and the transistors perform as dual-gate transistors which have their transconductance increase from g_m to $g_m + g_{mb}$. The 5-15% enhancement of the equivalent g_m leads to higher gain and lower noise figure.

IV. Implementation

A simplified SFBCG LNA circuit schematic is shown in Fig. 3. Output buffers (not shown) are added for testing. The input coupling capacitors are implemented by Metal-Insulator-Metal (MIM) capacitors that provide good linearity and small parasitic capacitance. The value is chosen as 40pF that sets the lower corner frequency at 100MHz. The gates of the foot NMOS transistors are biased at V_{DD} so the LNA can be duty-cycled in a pulse-based UWB system to save power. This also biases the foot NMOS transistors in the linear region as resistors and avoids a current source matching issue.

V. Experimental Results

The test chip is fabricated using STMicroelectronics $0.13\mu\text{m}$ CMOS technology. For comparison, the SFBCG LNAs with and without back-gate coupling are fabricated. The die photo is shown in Fig. 4. The chip occupies an area of $1.3 \times 2\,\text{mm}^2$ (including pads), and it is packaged in a 44-pin TQFP package and assembled on a test board. Wideband baluns are employed for both input and output single-ended to differential transformation. The simulated and measured S-parameter data are shown in Fig. 5-7. The experimental results show that the SFBCG LNA w/back-gate coupling has a peak gain of $13\,\text{dB}$ at 100MHz, which is $0.2\,\text{dB}$ greater than that of the LNA without back-gate coupling. The $3\,\text{dB}$ bandwidths of the LNAs are 930MHz and 960MHz individually. The input match is better than $-10\,\text{dB}$ from 50MHz to 830MHz for

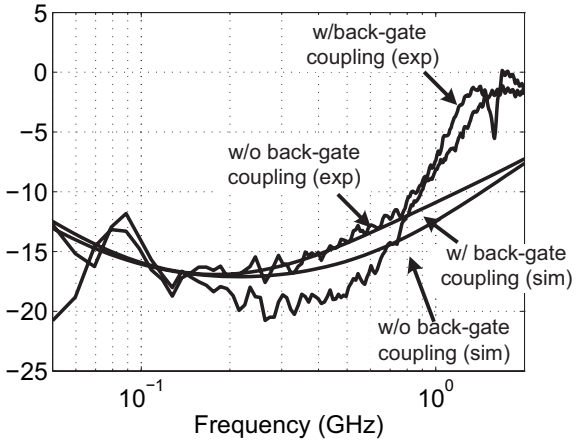

Fig. 5. Measured and simulated input match (s_{11}).

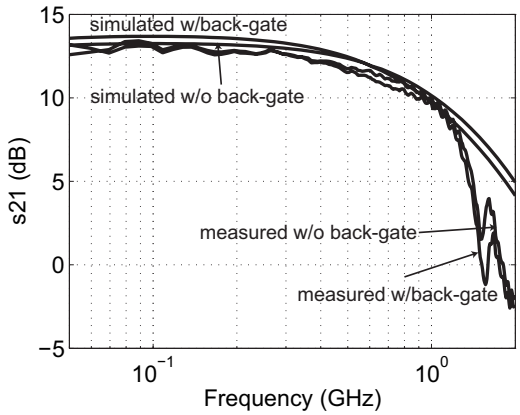

Fig. 6. Measured and simulated voltage gain (s_{21}). LNA with back gate coupling has higher gain.

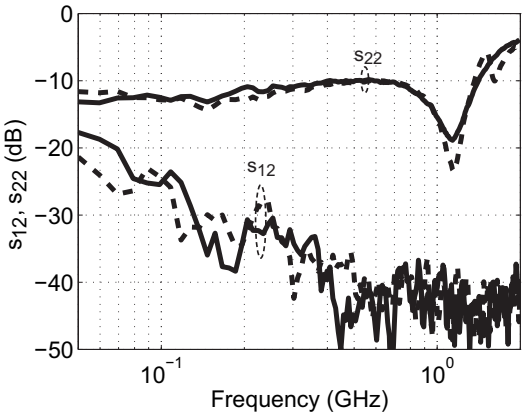

Fig. 7. Measured output match and isolation (s_{22},s_{12}).

	Technology	Bandwidth	Gain	NF	$IIP3$	Differential?	Input Match?	Power
Janssens [5]	0.5μm CMOS	$100-900\,$MHz	14.8 dB	3.3 dB	$-4.7\,$dBm	no	no	$3.4\,\text{mA}\times 3.3\text{V}$
Bruccoleri [1]	0.35μm CMOS	$50-900\,$MHz	11 dB	4.4 dB	14.7 dBm	no	yes	$1.5\,\text{mA}\times 3.3\text{V}$
Bruccoleri [4]	0.25μm CMOS	$2-1600\,$MHz	13.7 dB	2.5 dB	0 dBm	no	yes	$14\,\text{mA}\times 2.5\text{V}$
Adiseno [6]	0.18μm CMOS	$.8-1\,$GHz	26 dB	4.1 dB	4.5 dBm	yes	yes	$20\,\text{mA}\times 1.8\text{V}$
This work	0.13μm CMOS	$100-930\,$MHz	13 dB	4 dB	$-10.2\,$dBm	yes	yes	$0.6\,\text{mA}\times 1.2\text{V}$

TABLE I

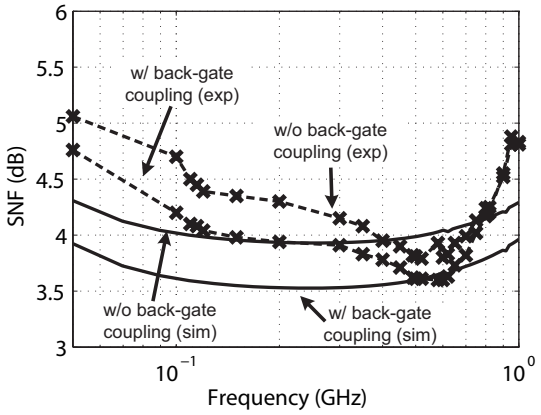

Fig. 8. Measured and simulated noise figure of the SFBCG LNAs.

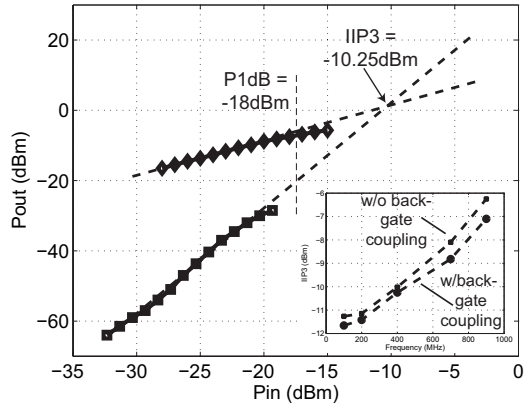

Fig. 9. Measured two-tone test at 400MHz for SFBCG LNAs with back-gate coupling. Inset: Measured $IIP3$ versus frequency.

the SFBCG LNA w/back-gate coupling and 890MHz for the SFBCG LNA w/o back-gate coupling. The S_{12} and S_{22} are comparable for the two cases. S_{12} is better than $-20\,\text{dB}$ and S_{22} is better than $-10\,\text{dB}$.

Fig. 8 shows the noise figure data of the two LNAs. As expected, SFBCG LNA w/back-gate coupling has a better noise performance over the one without. The minimum noise figures both happen at around 600MHz ($3.6\,\text{dB}$ and $3.8\,\text{dB}$) and the maximum at 950MHz ($4.81\,\text{dB}$ and $4.88\,\text{dB}$). The average noise figures from 100MHz to 1GHz are 4dB and 4.2dB individually.

Two-tone test for third-order intermodulation distortion is done for the two LNAs over the whole bandwidth and the one at 400MHz for SFBCG LNA w/back-gate coupling is shown in Fig. 9. The IIP3 is $-10.25\,\text{dBm}$ and the input 1-dB compression point is $-18\,\text{dBm}$. The inset shows $IIP3$ over frequency and SFBCG LNA w/o back-gate coupling has a slightly better linearity. Each LNA consumes 0.6mA of current (0.72mW at 1.2V) and the buffer draws 3mA.

Table I summarizes the measured performance and compares the design to recently published wideband LNAs.

VI. Conclusion

A wideband LNA combining shunt-feedback and common-gate topologies has been demonstrated. By directly coupling the input signal to the gate-source nodes of the devices without division, this LNA achieves a four-fold reduction in power consumption over the conventional shunt-feedback and common-gate amplifiers without compromising the noise performance. The approach has been verified experimentally in a $0.13\mu\text{m}$ CMOS technology.

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