A FULLY INTEGRATED LOW COST PACKAGED CMOS LOW NOISE AMPLIFIER FOR THE UWB RADIO

TU4C-4

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Abstract

A fully integrated low noise amplifier (LNA) has been designed in 0.25μm CMOS technology for the ultra-wideband (UWB) radio. The LNA operates in the 3.1 - 4.8GHz band. Within this band, the noise figure is less than 4.9dB, $|S_{11}| < -10.5$dB, $|S_{21}| > 8.5$dB, and IIP3 > -2.2dBm. The LNA core block dissipates 10 mA current from a 2-volt power supply. The designed LNA is packaged in a regular LQFP package and shown not to be too sensitive to the bonding wire length.

I. Introduction

Ultra-wideband (UWB) radio systems are defined as those with a 10dB bandwidth that exceed 20% of the center frequency or with a total bandwidth of more than 500MHz. The benefits of using the UWB radio are derived from its large bandwidths. Increasing the data rate by expanding the bandwidth is generally much more efficient than by resorting to higher order modulation schemes with sophisticated error control coding. In addition, its wide bandwidth provides the UWB signals with significant multipath diversity, resulting in greater robustness to fading.

The Federal Communication Commission (FCC) has recently approved the 3.1GHz - 10.6GHz band for UWB deployment. Because the U-NII bands (5.15GHz - 5.85GHz in the United States and 4.9GHz - 5.1GHz in Japan) lie right in the middle of the allocated spectrum, the UWB spectrum can be broken into two distinct and orthogonal bands that are free from interference: 3.1GHz - 4.8GHz and 6.0GHz - 10.6GHz. We subsequently refer to these two bands as the lower and upper UWB bands, respectively. Since operating at lower frequencies generally relaxes the implementation requirements, the initial deployment of the UWB systems will most likely use the lower UWB band [1][2].

One of the challenges in quantifying the performance of the UWB LNA is in defining its bandwidth. To define the frequency range where the LNA is useful, we first review the main functions of the LNA. The primary purpose of the LNA is to provide enough gain to overcome the noise of the subsequent stages while ensuring that the noise figure is adequately small. We define sufficiently high gain (in terms of $|S_{21}|$) to be >8dB and sufficiently low noise figure as <5dB. Achieving a flat $|S_{21}|$ over the lower UWB band is unnecessarily stringent, since the variations in the frequency gain caused by the LNA are indistinguishable from the distortions caused by the large number of multipaths in the UWB propagation channel. Consequently, the performance after decoding in the digital domain is unaffected by the flatness of the gain, especially when the transmitted signal is an OFDM signal [1]. Another requirement is to present a 50Ω input impedance, which is particularly important if a passive filter precedes the LNA, since the transfer characteristic of this pre-select filter is sensitive to its termination. For a receiver operating in the lower UWB band, a pre-select filter is necessary to filter out the signals in the ISM and UNII bands. The bandwidth of our LNA, therefore, is defined as a frequency range where $|S_{21}| > 8$dB, $|S_{11}| < -10$dB, and NF < 5dB.

This paper describes the design and implementation of a packaged low-noise amplifier (LNA) with fully integrated on-chip matching network for UWB systems operating in the 3.1GHz - 4.8GHz band. The organization of this paper is as follows. Section II describes the design strategy and the proposed LNA structure. The measurement results and conclusions are presented in Sections III and IV, respectively.

II. Wideband Low Noise Amplifier

A. Input Power Matching

For maximum power transfer, the input of the wideband LNA should provide an impedance of typically 50Ω over the frequency band of interest. This is usually achieved by placing a matching network before the LNA core as shown in Fig. 1. Since our goal is to design an LNA that is fully integrated with no off-chip matching components, the package and pad parasitics are viewed as part of the LNA matching network. In addition, the choice of the matching network topology should not be sensitive to the length of the bonding wire, as it is often difficult to predict accurately.

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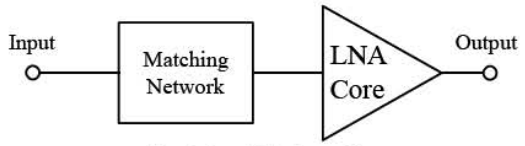

Fig. 1. Overall design architecture.

To determine the matching network and the impedance requirement of the LNA core, we first assume that the input impedance of the LNA chip is 50Ω as illustrated in Fig. 2. After accounting for the effect of the inductive package/bonding wire and the pad capacitance, the impedance of the remaining LNA that provides an overall input impedance of 50Ω is denoted as Z_B. For package/bonding wire inductance value of 3nH and pad capacitance value of 300fF assuming no ESD protection, the impedance Z_B at 4GHz consists of a positive resistive and a negative reactive term, which can be realized using a combination of a capacitor and a resistor (Fig. 3).

There are three different ways of implementing the required impedance Z_B as shown in Fig. 3. The drawback of the first realization (Fig. 3(a)) is that the noise figure increases substantially because of the voltage divider loss caused by the matching network. The second and third realizations have similar gain and noise characteristics. However, the third implementation (Fig. 3(c)) is less sensitive to the package/bonding wire inductance. Hence, the third configuration was chosen in our design.

At 4GHz, the capacitance in Fig. 3(c) is 1pF and the resistance is 150Ω. This matching network, which can be modeled as an equivalent series RLC circuit at 4GHz, has a quality factor of 1.5. The low quality factor suggests that the bandwidth of the matching network is sufficiently wide to support UWB signals in the lower UWB band.

B. Input Impedance of LNA Core

To design the LNA core to have a resistive input impedance of approximately 150Ω over the lower UWB band, a common-source stage with shunt feedback is employed as shown in Fig. 4. Although a common gate stage could have been used instead, the drawback is that achieving 150Ω input impedance would cause the gain to be small. In our common-source stage with shunt feedback, an inductor is placed in parallel at the input of the LNA core to compensate for the effects of the input capacitor and to ensure that the loop gain of the LNA core is sufficiently high over the band of interest. The LNA core input impedance can then be approximated as

$$Z_{core} \approx \frac{1}{g_m} + \frac{Z_F}{g_m Z_L} \quad (1)$$

where g_m is the amplifier transconductance, Z_F is the feedback impedance, and Z_L is the drain tank circuit impedance. The feedback impedance Z_F consists of the intrinsic gate-drain capacitance C_{gd} in parallel with the feedback resistance R_F (C_2 effect is negligible). To ensure that Z_{core} is approximately 150Ω over the frequency band of interest, the second term on the right-hand side of (1) should also be made approximately constant. This can be achieved by designing the drain tank circuit to resonate at a frequency below the lower UWB band, resulting in $Z_L \approx 1/(j\omega C_L + G_L)$, where C_L and G_L are the equivalent load capacitance and admittance, respectively. Since $Z_F = 1/(j\omega C_{gd} + G_F)$, where $G_F = 1/R_F$, Z_{core} in (1) becomes

$$Z_{core} \approx \frac{1}{g_m} + \frac{1/(j\omega C_{gd} + G_F)}{g_m/(j\omega C_L + G_L)} = \frac{1}{g_m}\left(1 + \frac{j\omega C_L + G_L}{j\omega C_{gd} + G_F}\right) \quad (2)$$

By selecting R_F and transistor width so that $G_F / C_{gd} \approx G_L / C_L$, Z_{core} can be made to be approximately 150Ω and independent of frequency. For sufficiently large loop gain, the transimpedance gain is approximately Z_F, which decreases with frequency. This reduction in gain, however, can be compensated by a second stage amplifier as described shortly.

C. Noise figure minimization

For a given input transistor width and power dissipation, the required inductance and feedback resistance values that

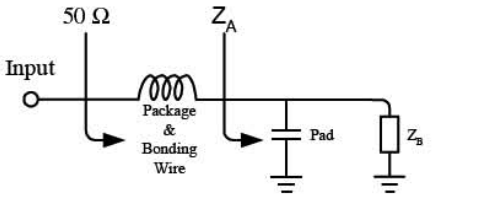

Fig. 2. Matching network.

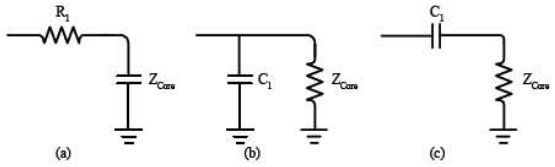

Fig. 3. Different choices for Z_B.

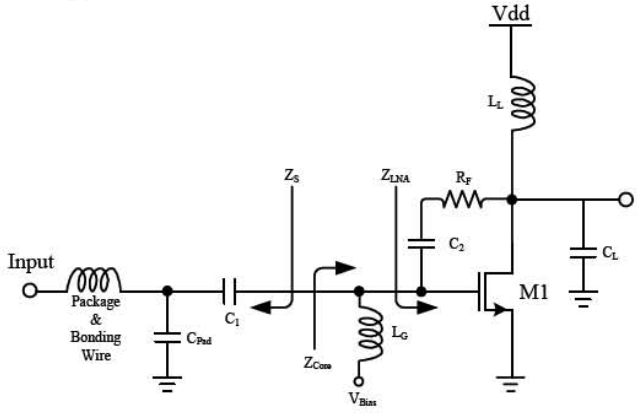

Fig. 4. First stage topology.

achieve the desired 150Ω input impedance can be calculated. Therefore, the only parameter available to minimize the noise figure for a given power dissipation is the width of the transistor.

The effect of all the noise sources on the noise figure including the on-chip inductors and the transistor drain and gate noise has been solved analytically. The two dominant noise sources were found to be the drain noise and the thermal noise from the on-chip inductor at the gate. For a given power consumption, increasing the width of the transistor reduces the drain noise because of the increased g_m. However, a larger g_m increases the gate-source capacitance C_{gs}, which in turn decreases the required inductance at the gate, causing the noise contributed by the inductor to increase for a fixed inductor quality factor. This trade-off is illustrated in Fig. 5, which plots the normalized input referred noise as a function of the transistor width at 3, 4, and 5GHz. The minimum in the three plots is relatively broad and occurs at approximately similar transistor widths. Based on Fig. 5, a transistor width of 160μm is selected in our design.

D. Overall LNA design

As discussed earlier, the transimpedance gain of the LNA core is approximately Z_F and, consequently, drops with frequency. Thus, to achieve reasonable gain values at higher frequencies, a second amplifier stage is added as shown in Fig. 6. In addition to compensating for the drop in gain at higher frequencies, the second amplifier serves as a buffer to drive the pad capacitance, bonding and package parasitics, and the output resistive load of 50Ω. The second amplifier, which is designed to be a tuned cascode stage, dissipates the same power as the LNA core. In an actual receiver, the requirements of the second amplifier stage are much more relaxed since it does not need to drive an off-chip load. Thus, its power dissipation can be significantly reduced.

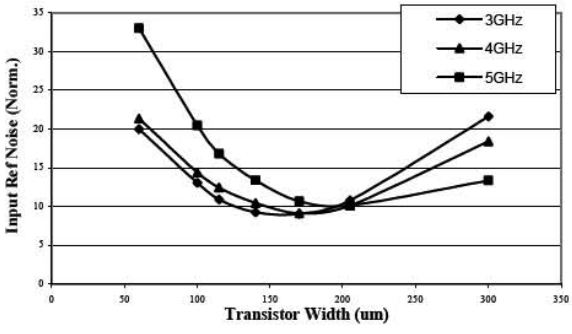

Fig. 5. Input referred noise as a function of transistor width.

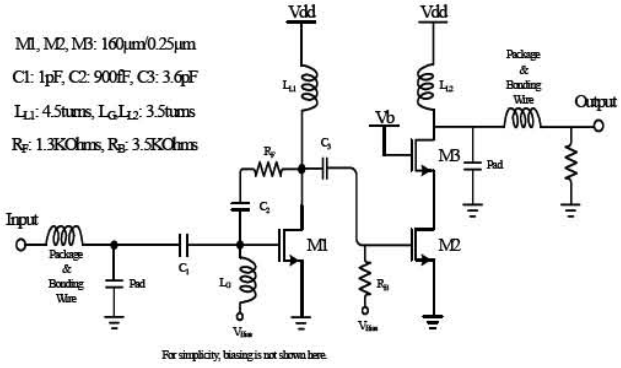

Fig. 6. Complete topology of the proposed LNA.

III. Measurement Results

Our UWB LNA has been fabricated in 0.25μm CMOS technology and packaged in regular leaded LQFP package. Fig. 7 shows a micrograph of the die. The die size is 1.3mm x 1.1mm.

The magnitude of the measured S_{11} of the LNA using 50Ω reference impedance is shown in Fig. 9. The frequency range where $|S_{11}| < -10$dB is very broad, ranging from 1.65GHz to 10.8GHz. For the range of 2-4nH input bonding wire inductance, S_{11} changes 1dB. The magnitude of S_{21} is also plotted as a function of frequency in Fig. 9. In the 3.1 - 4.8GHz band, the magnitude of S_{21} exceeds 8.5dB. However, $|S_{21}|$ peaks at around 2.5GHz, because as described earlier, the load tank is designed to resonate at a lower frequency in order to have approximately constant input impedance over the frequency band of interest. In actual receiver architecture, the second stage can be tuned to a higher frequency to make the gain flatter. The contribution of this stage to the overall noise figure is small because of the first stage gain. Output matching is not wideband thus S_{22} is not shown. S_{12} is less than –40dB over the band of interest.

The gain and input matching outside the lower UWB band suggest that our LNA can be used to simultaneously support other communication standards (e.g., 802.11b and 802.11a) in addition to UWB. This feature can be used to design a multimodal receiver; this will help in smooth migration to future generation systems and also intercontinental roaming. The performance of the LNA is not as good as some other published work for those systems, but having them with UWB is the unique feature of our design.

The measured NF as a function of frequency is shown in Fig. 10. The NF is less than 5dB for the frequencies between 2.2-5GHz. In the lower UWB band, the NF is less than 4.9dB. IIP3 (input referred third order intermodulation

Table I
LNA Performance

Input Matching bandwidth (|S11|<-10dB)	1.7 – 10.8 GHz
Gain bandwidth (|S21|> 8dB)	1.65 – 6.5 GHz
Noise Figure (3.1-4.8 GHz)	4.2 – 4.9 dB
IIP3 (3.1-4.8 GHz)	-2.2 – +5 dBm
$XIIP3_{802.11a}$ (5.2 & 4.8 GHz)	> -1 dBm
$XIIP3_{802.11b}$ (2.4 & 3.1 GHz)	> -4 dBm
ICP-1dB (3.1-4.8 GHz)	-12 – -3 dBm
$XICP\text{-}1dB_{802.11a > UWB}$	-9.83 dBm
$XICP\text{-}1dB_{802.11b > UWB}$	-18 dBm
Technology	TSMC 0.25μm CMOS
Die Area	1.5 mm^2
LNA Core Power (2-Volt supply)	20 mW

Table II
Performance of Some Other Designs for Comparison

Reference	[4]	[5]	[6]	[7]	This work
Frequency band (GHz)	0.8 – 2	5.18 – 5.825	3 – 10	3 – 10	3.1 – 4.8
Measured S11 (dB)	-41 – -9.2	-20 – -11	-37 – -10	-14 – -10	-13.2 – -10.5
Measured Gain (dB)	19.2 – 20.2	17.95 – 18.82	9.3	21	8.5 – 12.3
Measured NF (dB)	3.1 – 3.9	3.9 – 4.2	4 – 9	2.5 – 4.2	4.2 – 4.9
Measured IIP3 (dB)	-4.5 – -3	-3.5	-8 – -6	>-5.5	-2.2 – 5
Power (mW)	45	26.4	9	30	20
Technology	RF Si-bipolar	BiCMOS	0.18μm CMOS	SiGe-bipolar	0.25μm CMOS
Fully Integrated	No	Yes	No	No	Yes
Package type	Not Packaged	VFQFPN	Not Packaged	Not Packaged	52-LQFP

intercept point) and ICP-1dB (input referred 1-dB compression point) are plotted as a function of frequency in Fig. 10. In the frequency band of interest, IIP3 and ICP-1dB exceed -2.5dBm and -10dBm, respectively. In addition, we measured the cross IIP3 between a tone inside the band of interest and the closest interference signals, which are the ISM and U-NII bands (i.e., 2.4GHz and 5.2GHz). We also measured the amount of interference level at these frequencies that would cause the small signal gain at 4GHz to drop by one dB; we called this value XICP-1dB (Table 1). These values can be used to design the pre-select filter.

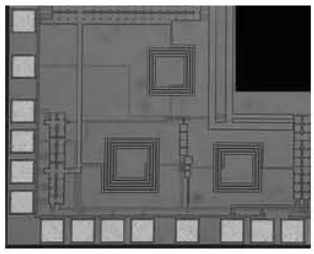

Fig. 7. Chip micrograph.

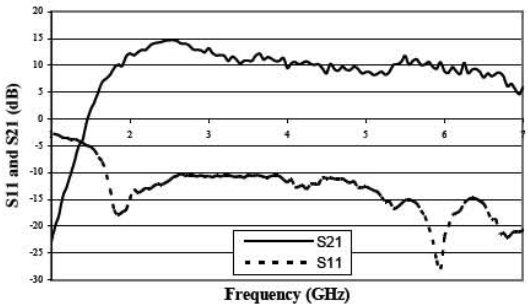

Fig. 8. Measured S-parameters.

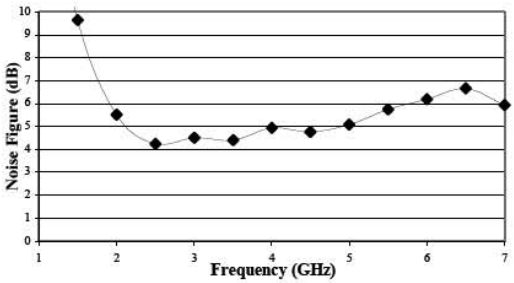

Fig. 9. Measured noise figure.

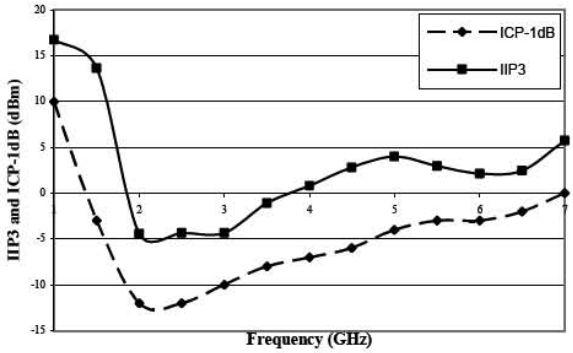

Fig. 10. Measured IIP3 and ICP-1dB for different carrier frequencies.

IV. Conclusion

We have implemented a packaged fully integrated LNA to receive the lower UWB band of 3.1GHz - 4.8GHz. Compared to existing wideband designs found in the literature, our design covers a much wider bandwidth and requires no off-chip matching component, while achieving similar performance in CMOS technology (Table II).

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