A 2.3mW Baseband Impulse-UWB Transceiver Front-end in CMOS

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Abstract

A highly-integrated, flexible, baseband impulse-UWB transceiver front-end comprising a 1-bit, 1.92 GSample/s A/D conversion, 50Ω input matching and 0-42dB variable gain, control logic, 60MHz oscillator, and a pulse transmitter was implemented in 2.52mm^2 of a standard 0.13µm CMOS process with power consumption of 1.8mW (RX) and 0.5mW (TX) at 10Mpulses/s with a 1.1V supply.

Introduction

In the United States, the FCC specification for Ultra-Wideband radio constrains operating power to limits similar to Part 15, the minimum bandwidth to 500MHz, and the peak to average ratio, but does not dictate the physical signaling[1]. This opens to the door to non-traditional radio design, such as the use of short "baseband" impulses on the order of a nanosecond which spread energy over a large bandwidth. The nature of impulse signaling promises lower cost, lower power architectures due to a simplified analog front-end design which lacks the need for carrier frequency synthesis and translation. The majority of attention has been focused on commercial UWB communication from 3 to 10GHz, but operation from dc to 960MHz is also allowed for imaging, ranging and communication systems such as surveillance or sensor networks. Low frequency operation is desirable for better material penetration and transmit distances, ease of design, and lower power consumption, but comes at the cost of increased passive and antenna size and interference from pre-existing users. A radio for these applications has a relatively low data rate (~100kbps), the ability to perform ranging or channel sounding, and aggressively targets low power consumption.

System Architecture and Results

The work presented in this paper achieves power consumption of 2.3mW, over 50x lower than the front-end reported in [2] and comparable to the power in [3], a simpler analog correlation-based approach, for a similar target application. This transceiver employs a "mostly-digital" architecture, shown in Fig. 1. The ADC is moved as close to the antenna as possible, after matching and gain, and signal processing occurs in the digital domain. Sampling occurs in a time-interleaved bank of 32 ADC's, driven by the delay line in a delay-locked loop (DLL) driven by a crystal oscillator reference. Digital logic controls reception timing and pulse generation. The transceiver only requires an external resistor for bias and LC tank for harmonic oscillation. The backend digital processing is implemented off-chip. Transceiver operation is also illustrated in Fig. 1. The further step of duty-cycling the front-end circuits saves more power at low pulse rates and has not been seen in reported literature. Additional flexibility for experimentation is provided: modulation may be 2-PAM, 2-PPM, or both, gain may vary from 0dB to 42dB, and operation may be communication or RADAR.

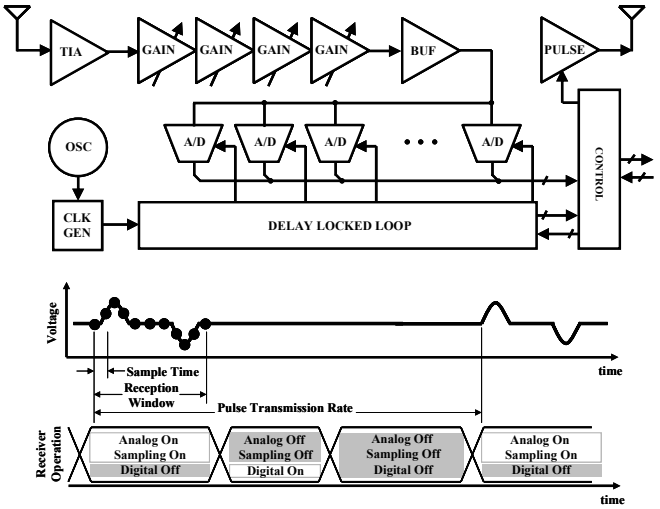

Fig. 1.Overview of transceiver architecture and operation.

Placing the ADC close to the antenna can incur a critical power penalty due to high-speed requirements. Simulation results show that, in the presence of large interferers, 1-bit sampling performs adequately and reduces power concerns[4]. The presence of interference also reduces the noise figure design constraints, which helps to lower power consumption. A 10mV σ_{VOS} was targeted and measurements indicate that that all comparators switch within a 30mV range.

The ADC sampling clock is generated by phases from the DLL, fed by a third-overtone Pierce crystal oscillator circuit. The oscillator runs at 60MHz with 23ps cycle-to-cycle jitter and is pullable +/-10PPM with an on-chip digital capacitor array. The delay line length was chosen at 32 as a compromise between oscillator frequency and delay tap jitter. A current-starved inverter is employed as the delay cell as it has no static bias current and does not require conversion back to CMOS logic levels. Per tap jitter was measured to be better than 15ps relative to the first tap with +/-100ps delay accuracy. To accommodate duty-cycling, the charge pump was modified to isolate the delay control voltage during non-operation to limit leakage. Less than 2% accuracy variaton and no change in jitter performance was seen down to 2% update duty cycle. Of final note is that the delay cell was designed to generate both a low to high and high to low transition for every incoming edge, to preserve the duty-cycle and prevent pulse-swallowing inside the delay line.

For the gain stages a differential topology was chosen to reject substrate/supply noise in spite of the power penalty. In addition to a large gain-bandwidth product, these amplifiers are expected to have fast overload recovery and be relatively linear and memoryless. Offset cancellation, usually realized with low-frequency feedback, was implemented in a feed-forward manner to allow duty-cycling thus requiring foreground calibration prior to operation. All blocks are

trimmable +/-20mV with a stepsize less than 1mV. Duty-cycling is achieved by gating the bias and isolating the input to avoid long recovery transients. The transimpedance amplifier (TIA) provides an input match of < -10dB S11 to 50Ω over 600MHz and 12dB of gain with a 12dB noise figure. The variable gain blocks produce -2.5dB to 7.5dB per stage and overall gain varies from 0dB to 42dB with -3dB at 200MHz, -10dB at 350MHz and < 10dB at 900MHz (large cellphone interferers exist around 900MHz.) Settling occurs within 6ns of turn-on during duty-cycling. Fig. 2 shows the S11 matching and overall gain.

Pulse transmission is achieved with an H-bridge (differential inverters) and pulse width may be varied from 1ns to 2ns with an edge rate between 150ps to 750ps. To demonstrate system functionality, 2ns pulses with 750ps edges were encoded with an 11x11 concatenated Barker code using 2-PAM and sent through a TEM horn to a receive TEM horn at 1meter, sampled and post-processed. The transmit pulses and receive data correlation are shown in Fig. 3.

Table 1 summarizes power and area for each block of the transceiver. For non-duty-cycled operation (100% activity) at 30Mpulses/s, the RX block consumes 3.5mA and TX 1.8mA. A die photo is shown in Fig. 4.

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References

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TABLE I. SUMMARY OF AREA AND POWER CONSUMPTION

System Parameters	1.1V; 60MHz (1.92GSamples/s), Duty-Cycled at 10Mpulses/s	
	Block Area	Current Usage
Trans. Imp. Amp	0.33 mm^2	354 µA
Var. Gain Stages	0.20 mm^2	198 µA
ADC Buffer/Driver	0.12 mm^2	87 µA
ADC Slicers	0.10 mm^2	148 µA
Delay Locked Loop	0.16 mm^2	291 µA
Clock Buffer	0.02 mm^2	71 µA
Oscillator	0.33 mm^2	79 µA
Control Logic	0.24 mm^2	252 µA
Bias	0.06 mm^2	188 µA
Receiver: Total	2.04 mm^2	1668 µA
Transmitter: Total	0.48 mm^2	464 µA

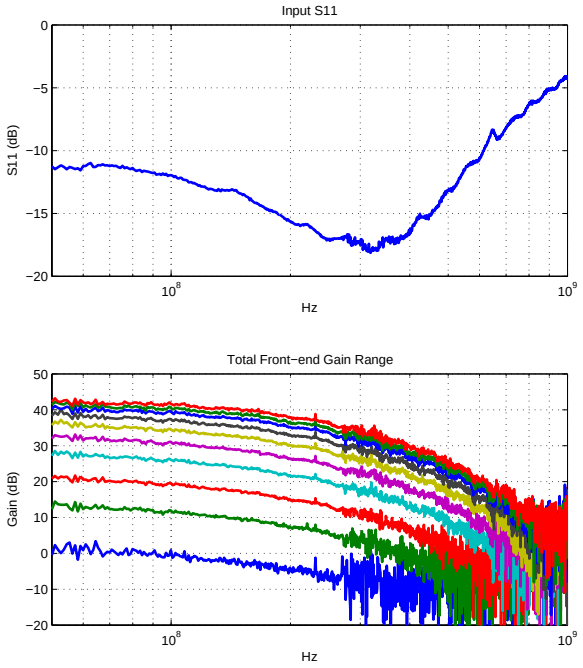

Fig. 2. Gain stages : Input match, and variable gain range.

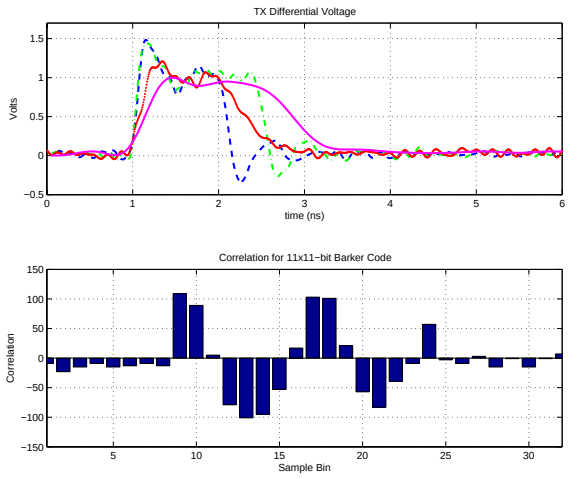

Fig. 3. Transmit pulse and received correlation result.

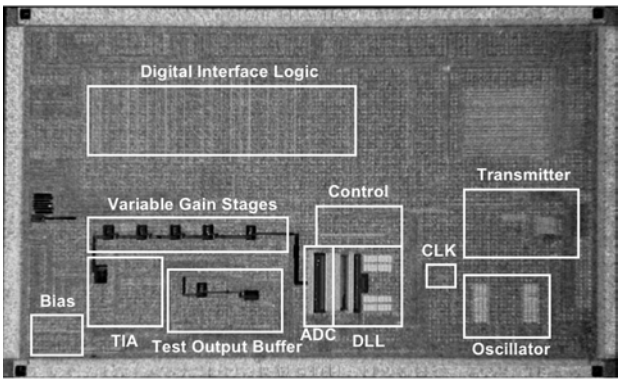

Fig. 4. Die photo of transceiver front-end.