Wideband CMOS Low Noise Amplifier Design Based On Source Degeneration Topology

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Abstract

A design methodology for wideband CMOS low noise amplifier (LNA) with source degeneration is presented. By allowing an arbitrary source degeneration and employing a general input matching network, the minimum noise figure of the proposed wideband CMOS LNA can be made independent of the transistor width by properly choosing the source degeneration reactance. This result shows that the proposed topology is effective as a wideband LNA, since the same transistor can be used to achieve the minimum noise figure at all frequencies of interest. The transistor width simply affects the gain of the LNA at the cost of power dissipation. These results apply uniquely to CMOS LNA, as they are derived from a quasi-static MOSFET model. To validate these design concepts, a wideband LNA was realized in 0.25μm CMOS technology. The measured noise figure ranges from 2.7-3.7dB over 3.2-4.8GHz with power consumption of 20mW. A close agreement with the theoretical results is observed.

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I. INTRODUCTION

The primary objective in the design of the LNA is to achieve sufficiently large gain and low noise figure to suppress the additive noise at the subsequent stages. In most systems, this objective should be achieved while constraining the LNA input to provide an impedance of generally 50Ω to avoid signal distortion caused by impedance mismatch. To provide a 50Ω input termination, common wideband LNAs use either a resistive termination by connecting a resistor in parallel at the input of the amplifier or employ a negative parallel resistive feedback. In both approaches, the presence of the resistor has a deleterious effect on the amplifier's noise figure. Furthermore, the latter architecture suffers from potential instability [1].

In narrowband systems, low noise figure is achieved by employing an inductive source degeneration to present a 50Ω input resistance without the resistive thermal noise. To satisfy the input power matching condition, another inductor is placed at the gate of the MOSFET to resonate at the desired frequency, which is typically at the carrier frequency [2][3]. Although low noise figure can be achieved, this technique is only suitable for narrowband applications as the optimal transistor width is a function of the resonant frequency.

This paper extends the design approach for narrowband LNA with source degeneration to wideband systems. The main difference is that in the proposed approach an arbitrary source degeneration and a general lossless matching network at the gate are employed. When the noise figure of the proposed LNA architecture is minimized constrained to input power matching condition, our analysis shows that the minimum noise figure can be made independent of the transistor width by properly choosing the source degeneration reactance. This result applies uniquely to CMOS LNA, since the analysis is based on the quasi-static MOSFET model. Our analysis result suggests that the proposed architecture is effective as a wideband LNA, since the minimum noise figure can be achieved at all frequencies of interest using the same transistor. The transistor width simply affects the gain of the LNA at the cost of power dissipation. To validate this concept, a wideband LNA has been designed in 0.25um CMOS at the target frequency range of 3.2GHz to 4.8GHz.

The paper is organized as follows. Section II presents the fundamental noise theory for a common source MOSFET amplifier with source-degeneration. Design considerations for the wide-

band LNAs are presented in Section III. Section IV presents the LNA implementation issues and a detailed discussion of the experimental results. Conclusions are drawn in Section V.

II. NOISE THEORY FOR MOSFET AMPLIFIERS

A. Two-Port Circuit Model of Noisy MOSFET

The general block diagram of a LNA is shown in Fig. 1(a), where two identical MOSFETs M1 and M2 form a cascode amplifier and the input and output matching networks are assumed lossless. The advantage of this topology is that the Miller effect at the gate-drain capacitance in M1 is small, and M2 has a high output impedance at its drain, improving reverse isolation and as a result the stability of the LNA. In this paper the quasi-static MOSFET model is employed to account for the high-field effects in short-channel devices [4]. Equation for the drain current is given by

$$I_d = \begin{cases} 2\nu_{sat} C_{ox} W \dfrac{(V_{od} - V_{ds}/2) V_{ds}}{(V_{ds} + L\varepsilon_{sat})}, & V_{ds} \le V_{dsat} \\ \nu_{sat} C_{ox} W \dfrac{V_{od}^2}{V_{od} + L\varepsilon_{sat}} \quad , & V_{ds} \ge V_{dsat} \end{cases} , \tag{1}$$

where W and L are the gate width and length; C_{ox} is the gate oxide capacitance per unit area; and v_{sat} ($=\mu_{eff}\varepsilon_{sat}/2$) is the saturation velocity with μ_{eff} and ε_{sat} denoting the effective electron mobility and the saturation electric field, respectively. In (1), V_{od} ($=V_{gs}$-V_{th}) is the gate overdrive voltage, V_{gs} is the gate-source voltage, V_{th} is the threshold voltage, V_{ds} is the drain-source voltage, and V_{dsat} is the drain-source saturation voltage, which is given by

$$V_{dsat} = \frac{V_{od}}{V_{od} + L\varepsilon_{sat}}, \tag{2}$$

Differentiating (1) in the saturation region with respect to V_{gs}, and in the linear region with respect to V_{ds} when V_{ds}=0 yields the ac characteristics of MOSFET, i.e., transconductance g_m and the zero-bias drain conductance g_{d0}.

$$g_m = 2\nu_{sat} C_{ox} W \left[\frac{\rho(1 + \rho/2)}{(1 + \rho)^2}\right], \tag{3}$$

$$g_{d0} = 2\nu_{sat} C_{ox} W \rho \quad , \tag{4}$$

where ρ (= $(V_{gs}-V_{th})/L\varepsilon_{sat}$) is referred to as the normalized gate overdrive. Another important design parameter is the gate-source capacitance C_{gs}, which is given by

$$C_{gs} = \frac{2}{3}C_{ox}WL \tag{5}$$

Fig. 1(b) presents the noisy small-signal model of the cascode amplifier block in Fig. 1(a), where the series-feedback at the source of M1 is modeled as $Z_s = jX_s$ and the admittance between the gate and source of M1 is $Y_f = jB_f\ (=j\omega C_{gs})$. In this paper the noise of MOSFET consists of the induced gate noise i_g and the channel noise i_d [5]. These current noises are partially correlated because they share a common origin and possess a power spectral densities (PSD) as given by

$$S_{i_g}(\omega) = 4kT\frac{\delta\omega^2 C_{gs}^2}{5g_{d0}}, \tag{6}$$

$$S_{i_d}(\omega) = 4kT\gamma g_{d0}, \tag{7}$$

$$S_{i_g i_d}(\omega) = c\sqrt{S_{i_g}(\omega)S_{i_d}(\omega)}, \tag{8}$$

where k (= 1.38x10^{-23} J/K) is the Boltzmann constant, T is the absolute temperature, δ and γ are the coefficients of the channel and gate noise and c is referred to as the correlation coefficient. In this paper, γ, δ and c are assumed 2.5, 5 and j0.395, respectively [6].

To systematically analyze the signal and noise behavior of the cascode amplifier with source-degeneration, a noisy ABCD matrix for the first and second stages of the cascode amplifier are, respectively, given by [7][8]

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} + \begin{bmatrix} e_{n1} \\ i_{n1} \end{bmatrix} = \begin{bmatrix} 0 & -jX_s - \dfrac{(1-X_sB_f)}{g_m} \\ 0 & \dfrac{-jB_f}{g_m} \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}, \tag{9}$$

$$\begin{bmatrix} V_2 \\ I_2' \end{bmatrix} + \begin{bmatrix} e_{n2} \\ i_{n2} \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{1}{g_m} \\ 0 & \left(1+\dfrac{jB_f}{g_m}\right) \end{bmatrix} \begin{bmatrix} V_2 \\ -I_3 \end{bmatrix}, \tag{10}$$

where $I_2 = -I_2'$ and

$$\begin{bmatrix} e_{n1} \\ i_{n1} \end{bmatrix} = \begin{bmatrix} jX_s & \dfrac{(1-X_sB_f)}{g_m} \\ 1 & \dfrac{jB_f}{g_m} \end{bmatrix} \begin{bmatrix} i_{g1} \\ i_{d1} \end{bmatrix}, \tag{11}$$

$$\begin{bmatrix} e_{n2} \\ i_{n2} \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{1}{g_m} \\ 1 & \dfrac{jB_f}{g_m} \end{bmatrix} \begin{bmatrix} i_{g2} \\ i_{d2} \end{bmatrix}. \tag{12}$$

In (11) and (12), the subscript *i* refers to the *i*-th stage of the cascode amplifier. In this paper, M1 and M2 are assumed to be of equal size so that they share the common ac characteristics and identical (but independent) noise statistics. Referring all noise sources to the input of the cascode amplifier, the equivalent voltage and current noise vector is given by

$$\begin{bmatrix} e_n \\ i_n \end{bmatrix} = \begin{bmatrix} e_{n1} \\ i_{n1} \end{bmatrix} + \begin{bmatrix} 0 & jX_s + \dfrac{(1-X_sB_f)}{g_m} \\ 0 & \dfrac{jB_f}{g_m} \end{bmatrix} \begin{bmatrix} e_{n2} \\ i_{n2} \end{bmatrix}. \tag{13}$$

Using the gate noise PSD, drain noise PSD, and their cross-PSD (as given in (6)-(8)), the noise correlation matrix M can be obtained by taking the expectation of the noise vector (as given in (13)) and its Hermitian transpose [8], i.e.,

$$M = E\left\{ \begin{bmatrix} e_n \\ i_n \end{bmatrix} \begin{bmatrix} e_n \\ i_n \end{bmatrix}^H \right\} = S_{i_g} \begin{bmatrix} m_{11} & m_{12} \\ m_{12}^* & m_{22} \end{bmatrix}, \tag{14}$$

where

$$m_{11} = |c|^2\left[X_s - \sqrt{\frac{5\gamma}{\delta(\alpha|c|)^2}}\frac{(1-X_sB_f)}{B_f}\right]^2 + (1-|c|^2)X_s^{\;2} \quad , \tag{15}$$

$$+\left(1+\sqrt{\frac{5\gamma}{\delta\alpha^2}}\right)\left(\frac{\omega}{\omega_T}\right)^2\left[\left(X_s - \frac{1}{B_f}\right)^2 + \left(\frac{g_m X_s}{B_f}\right)^2\right]$$

$$m_{12} = j|c|^2\left(1+\sqrt{\frac{5\gamma}{\delta(\alpha|c|)^2}}\right)\left[X_s - \sqrt{\frac{5\gamma}{\delta(\alpha|c|)^2}}\frac{(1-X_sB_f)}{B_f}\right] + j(1-|c|^2)X_s$$

$$+\left(1+\sqrt{\frac{5\gamma}{\delta\alpha^2}}\right)\left(\frac{\omega}{\omega_T}\right)^2\left[\frac{g_m X_s}{B_f} + j\left(X_s - \frac{1}{B_f}\right)\right]$$

$$m_{22} = |c|^2\left(1+\sqrt{\frac{5\gamma}{\delta(\alpha|c|)^2}}\right)^2 + (1-|c|^2) + \left(1+\sqrt{\frac{5\gamma}{\delta\alpha^2}}\right)\left(\frac{\omega}{\omega_T}\right)^2$$

where, from (3) to (4),

$$\alpha = \frac{g_m}{g_{d0}} = \frac{1+\rho/2}{(1+\rho)^2}, \tag{16}$$

$$\omega_T = \frac{g_m}{C_{gs}} = \frac{3\nu_{sat}}{2L}\left[1 - \frac{1}{(1+\rho)^2}\right], \tag{17}$$

in which (17) is commonly known as the angular cut-off frequency. Note that in (16) and (17), both α and ω_T are dependent on ρ only for a given L.

B. Expressions for four noise parameters

To derive the system noise figure, the noise parameters are first computed, i.e., the minimum noise figure F_{min}, the noise resistance R_n, and the optimum admittance Y_{opt} (=G_{opt}+jB_{opt}). With M specified in the preceding section, the noise parameters can be determined by [9]

$$F_{min} = 1 + \frac{S_{i_g}}{2kT}\left(\Re e(m_{12}) + \sqrt{m_{11}m_{22} - (\Im m(m_{12}))^2}\right), \tag{18}$$

$$Y_{opt} = \frac{\sqrt{m_{11}m_{22} - (\Im m(m_{12}))^2} + j\Im m(m_{12})}{m_{11}} \quad , \tag{19}$$

$$R_n = \frac{S_{i_g} m_{11}}{4kT} \quad . \tag{20}$$

Substituting (14) into (18), (19), and (20) and making the reasonable approximation of neglecting the high order terms of ω/ω_T, since MOSFETs typically operate at frequencies well below the cut-off frequency (i.e., $\omega/\omega_T \ll 1$), the noise parameters become

$$F_{min} = 1 + \frac{2\omega}{\omega_T}\sqrt{\frac{\delta\gamma}{5}(1-|c|^2)}, \tag{21}$$

$$R_n = \frac{\gamma}{\alpha^2 g_{d0}}[1 - 2u_1\chi^2 + (u_1^2 + u_2^2)\chi^4], \tag{22}$$

$$Y_{opt} = B_f\left[\frac{u_2 + j(u_3\chi^2 - u_1)}{1 - 2u_1\chi^2 + (u_1^2 + u_2^2)\chi^4}\right], \tag{23}$$

where we define the resonance factor as

$$\chi = X_s B_f = X_s \omega C_{gs} = \left(\frac{2}{3}\omega C_{ox} L\right) X_s W \tag{24}$$

and the coefficients $\{u_j\}$ (for $j \in \{1, 2, 3\}$) are given by

$$\begin{aligned} u_1 &= 1 + \sqrt{\frac{\delta(\alpha|c|)^2}{5\gamma}} \\ u_2 &= \sqrt{\frac{\delta\alpha^2}{5\gamma}(1-|c|^2)} \\ u_3 &= 1 + 2\sqrt{\frac{\delta(\alpha|c|)^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma} \end{aligned} . \tag{25}$$

It is worth noting that as γ, δ, and c are constants (at least for the 0.25µm CMOS technology [10]), and $\{u_j\}$ (for $j \in \{1, 2, 3\}$) is independent of *W*. Furthermore, since ω_T is dependent on ρ only (assuming minimum *L*; see (17)), F_{min} is also independent of *W*. As explained shortly, this independence will become relevant in the design of wideband CMOS LNA.

C. Expression for noise figure given perfect power match

Having computed the four noise parameters and denoting the admittance of the matching network as seen by the amplifier as Y_{as} ($=G_{as}+jB_{as}$, as shown in Fig. 1), the noise figure *F* can be determined by [7]

$$F = F_{min} + \frac{R_n}{G_{as}}[(G_{as} - G_{opt})^2 + (B_{as} - B_{opt})^2]. \tag{26}$$

Perfect power matching occurs when Y_{as} is the complex conjugate of the amplifier's input admittance Y_a, i.e.,

$$Y_a = \left(\frac{g_m X_s}{B_f} + jX_s + \frac{1}{jB_f}\right)^{-1} \tag{27}$$

$$= B_f\left[\frac{\frac{\omega_T}{\omega}\chi^2 + j(1-\chi^2)}{1 - 2u_1\chi^2 + (u_1^2 + u_2^2)\chi^4}\right]$$

Substituting Y_{as} (=Y_a^*, as given in (27)) and the four noise parameters (as given in (21)-(23)) into (26) yields the noise figure of the LNA that achieves the input power match. After tedious but straightforward algebraic manipulations, the LNA noise figure given the input power match, which we denote as F_{match}, can be shown to be

$$F_{match} = F_{min} + \frac{\gamma}{\alpha}\frac{\omega^2}{\omega_T^2}\frac{(U_1^2 + U_2^2)}{U_3 U_4 U_5}, \tag{28}$$

where the set of polynomial of χ are $\{U_i\}$ (for $i \in \{1, \ldots, 5\}$), i.e.,

$$U_1 = -u_2 + \left(\frac{\omega_T}{\omega} + 2u_2\right)\chi^2 - \left[2\frac{\omega_T}{\omega}u_1 + u_2\left(1 + \frac{\omega_T^2}{\omega^2}\right)\right]\chi^2 + \frac{\omega_T}{\omega}(u_1^2 + u_2^2)\chi^2 \tag{29}$$

$$U_2 = (1-u_1) - (1-u_3)\chi^2 + \left[u_1^2 + u_2^2 - 2u_3 + u_1\left(1 - \frac{\omega_T^2}{\omega^2}\right)\right]\chi^4$$
$$-\left[u_1^2 + u_2^2 - u_3\left(1 + \frac{\omega_T^2}{\omega^2}\right)\right]\chi^6$$

$$U_3 = \chi^2$$

$$U_4 = 1 - 2\chi^2 + \left(1 + \frac{\omega_T^2}{\omega^2}\right)\chi^4$$

$$U_5 = 1 - 2u_1\chi^2 + (u_1^2 + u_2^2)\chi^4$$

As F_{min} and $\{u_j\}$ (for $j \in \{1, 2, 3\}$ are independent of W (as shown in the previous subsection), (28) suggests that F_{match} becomes a function of χ only when the bias voltage ρ and the operating frequency ω are specified. Since χ is proportional to the product of X_s and W (or C_{gs}) (see (24)), this dependency of F_{match} on χ only suggests that the LNA can be designed to satisfy the optimum χ that minimizes F_{match} regardless of W by appropriately selecting X_s. This is an important result for wideband CMOS LNA design because it means that, for any W chosen to satisfy a given power dissipation constraint, the LNA can achieve the minimum F_{match} over the frequency range of interest, since X_s can be adjusted to yield the optimum χ at each frequency. As this dependency of F_{match} on χ is derived for the quasi-static MOSFET model given in (1), this result that the minimum F_{match} can be achieved at all frequencies of interest is unique to CMOS.

III. DESIGN CONSIDERATIONS FOR WIDEBAND LNAS

The wideband LNA design objective is to choose the MOSFET parameters (i.e, size W and bias ρ) and the source degeneration reactance X_s that minimize the noise figure over a frequency band of interest subject to power dissipation and input power matching constraints. The matching network at the gate is not a design parameter, since it is determined given X_s, W, and ρ. In this section, the role of each design parameter is described.

As discussed in the preceding section, F_{match} (as in (28)-(29)) is a function of χ only when ρ and W are fixed. Fig. 2 plots F_{match} against χ for ρ ranging from 0.1 to 1 at 4GHz. For a specific ρ, the minimum F_{match} (which we denote as $F_{match,opt}$) is achieved at a particular χ (which we denote as χ_{opt}) as shown in Fig. 2. Since χ is proportional to the product of X_s and W (see (24)), the LNA can be designed to satisfy χ_{opt} independent of W by appropriately selecting X_s. Furthermore, regardless of how χ_{opt} varies with frequency, the LNA can achieve $F_{match,opt}$ at each frequency of interest by appropriately choosing X_s.

Although the proposed LNA is able to achieve $F_{match,opt}$ at all frequencies independent of W, the choice of W affects the LNA gain. From Fig. 1, the effective transconductance G_m given the input power match can be computed as

$$G_m = \frac{|I_3|}{|V_s|} = \frac{1}{2}\sqrt{\frac{\omega_T}{\omega Z_0 X_s}} = \frac{1}{2}\sqrt{\frac{2\omega_T C_{ox} L W}{3\chi Z_0}}, \tag{30}$$

where Z_0 is the characteristic impedance (or 50Ω). The last equality in (30) is obtained by using (24) to replace X_s. As is clear from (30), increasing W increases G_m. This increase in G_m, however, is at the expense of increasing power dissipation P_{wr} for a given ρ (or V_{od}) as can be seen from (1). Hence, the choice of W has no bearing on $F_{match,opt}$ but affects G_m and P_{wr}. The relation between G_m and P_{wr} is shown in Fig. 3(a) for different ρ (or $F_{match,opt}$) values at 4GHz. In Fig. 3(b), the increase in W as a function of P_{wr} is plotted.

When P_{wr} is fixed, the role of ρ is to affect the tradeoff between $F_{match,opt}$ and G_m. As can be seen from Fig. 2, increasing ρ gradually decreases $F_{match,opt}$. However, G_m is also decreased, because as ρ increases, W must be reduced to keep the drain current (and as a result P_{wr}) constant (see (1)), which in turn reduces G_m from (30). The dependency of $F_{match,opt}$ and G_m is illustrated in Fig. 4(a)-(c), which plot $F_{match,opt}$, F_{min} and G_m as a function of ρ at 3GHz, 4GHz, and 5GHz.

IV. MEASURED RESULTS

To validate the proposed wideband CMOS LNA design concept, a 3.2-4.8GHz LNA was implemented in TSMC 0.25μm CMOS technology. This frequency band is selected, as it represents the likely operating band of the first generation ultra-wideband (UWB) radio [11][12]. A complete schematic of the test system is illustrated in Fig. 5 and the die photo is shown in Fig. 6. The LNA was designed for a target power consumption of 20mW. As a good compromise between $F_{match,opt}$ and G_m, ρ is selected to be 0.4 (or equivalently Vgs=1V), which represents the knee region of the noise figure curves in Fig. 4. The corresponding transistor size is 80μm/0.24μm.

Having sized and biased the transistor, the next step is to design the source degeneration X_s that satisfies χ_{opt} over the frequency range of interest. As shown in Fig. 7, the optimal X_s turns out to be relatively flat over 3-5GHz. To reduce the complexity of the source degeneration, the optimal X_s was approximated with a 1nH inductor, which was realized using a bonding wire. Since the region near χ_{opt} is relatively flat as shown in Fig. 3, this approximation should not significantly increase the noise figure. After approximating the optimal X_s, the input matching network is designed to satisfy the input matching constraint. The input matching network is implemented partially off-chip to account for the bonding wire's inductance and the pad capacitance at the gate of M1 as shown in Fig. 5. The off-chip matching network consists of a series-capacitor cascaded

with an all-inductor pi-network; whereas the on-chip matching network is simply an inductor of 4nH, which was realized with 3.5 turns as shown by the spiral inductor on the right in Fig. 6. An additional on-chip inductor of 6nH, which was realized with 4.5 turn, is placed at the drain of M2 to center the output signal to the frequency band of interest.

Fig. 8 presents the simulated F_{min}, simulated $F_{match,opt}$, and the measured noise figure with experimental setup as in Fig. 5. Even with the approximation of the optimal X_s using an inductor at the source degeneration, a close agreement between the measured noise figure and simulated $F_{match,opt}$ is observed. The measured magnitude of S11 and available gain are shown in Fig. 9, in which the measured return loss of greater than 9dB is achieved. The available gain is around 7dB with a 3dB bandwidth between 3.2GHz to 4.8GHz. Fig. 10 shows the measured IIP3 of 4dBm where two-tone signals of equal power were applied at 4 and 4.05GHz to the LNA. Summary of the performance results are given and compared with other published wideband CMOS LNA work in Table I, which suggests that the LNA in this work outperforms other LNAs in terms of noise figure.

V. CONCLUSIONS

This paper presents a design methodology for the wideband CMOS LNA with source degeneration. Using the quasi-static MOSFET model, our analysis shows that the minimum noise figure can be made independent of the transistor width by properly choosing the source degeneration reactance. This result shows that the proposed topology is effective as a wideband LNA, since the same transistor can be used to achieve the minimum noise figure at all frequencies of interest. The transistor width simply affects the gain of the LNA at the cost of power dissipation. The transistor bias voltage affects the tradeoff between gain and the minimum noise figure. The results obtained in this paper apply uniquely to CMOS LNA, as the analysis are based on the quasi-static MOSFET model. To validate the proposed wideband CMOS LNA design concepts, a wideband LNA was implemented in 0.25µm CMOS standard technology. A close agreement (< 0.3dB) between measurement and analytical results were observed. The measured noise figure is 2.7-3.7dB and the available gain is 7dB while dissipating 20mW.

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TABLE 1. LNA PERFORMANCE SUMMARY AND COMPARISONS

	This work	[13]	[14]
Frequency (GHz)	3.2~4.8	3~5	3.1~10.6
Supply Voltage (V)	2.5	N/A	N/A
S11 (dB)	-9.5~-15	-8~-14	-10~-37
IIP3 (dBm@GHz)	4@4	-4.7@2.5	-6.7@6
Noise Figure (dB)	2.7~3.7	4~5	4~9.6
Gain (dB)	7(Av)	13	9.2
Power (mW)	20	75	9
Technology	0.25μm CMOS	0.18μm CMOS	0.18μm CMOS

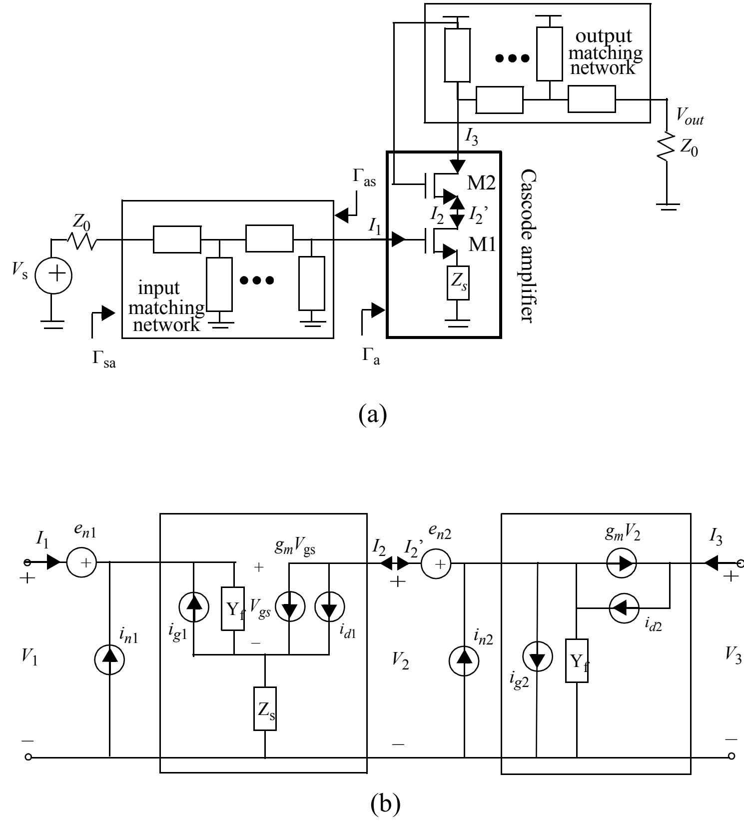


Fig. 1. LNA with reactive degeneration (a) block diagram, (b) noisy small-signal model of the cascode amplifier.

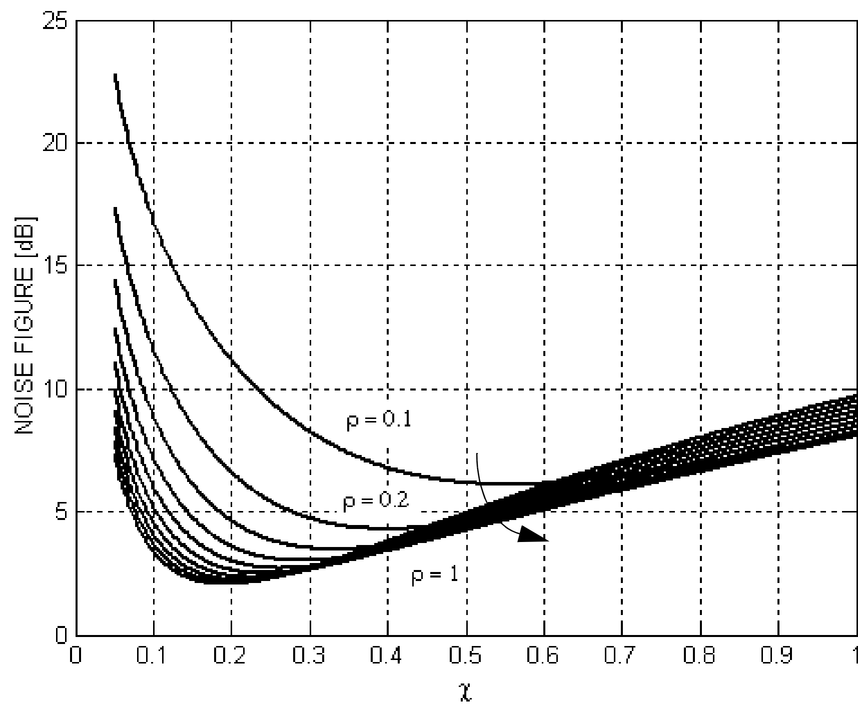
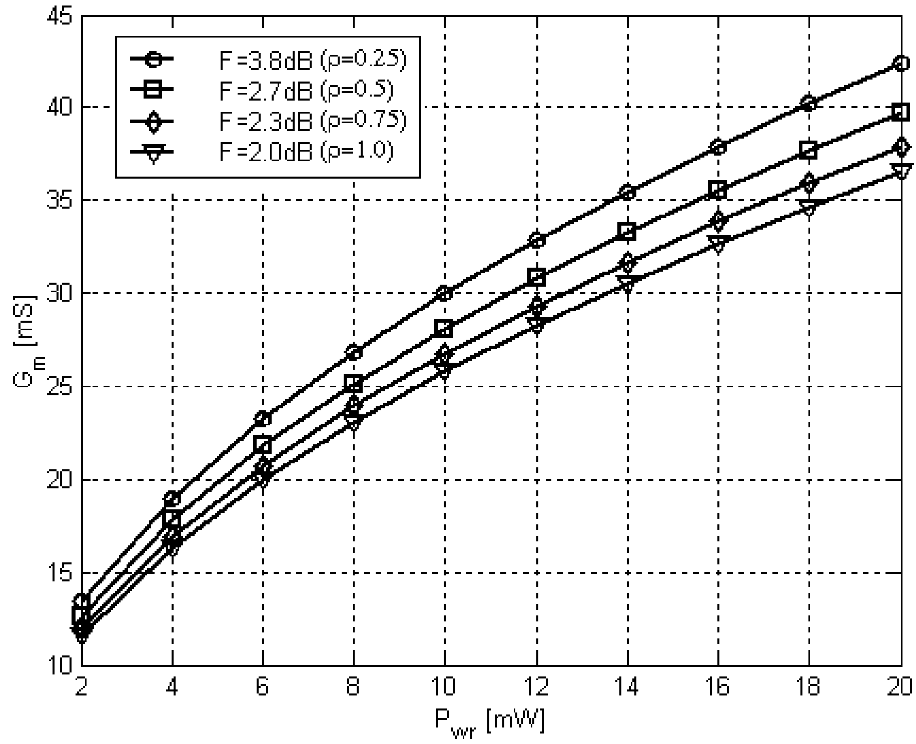
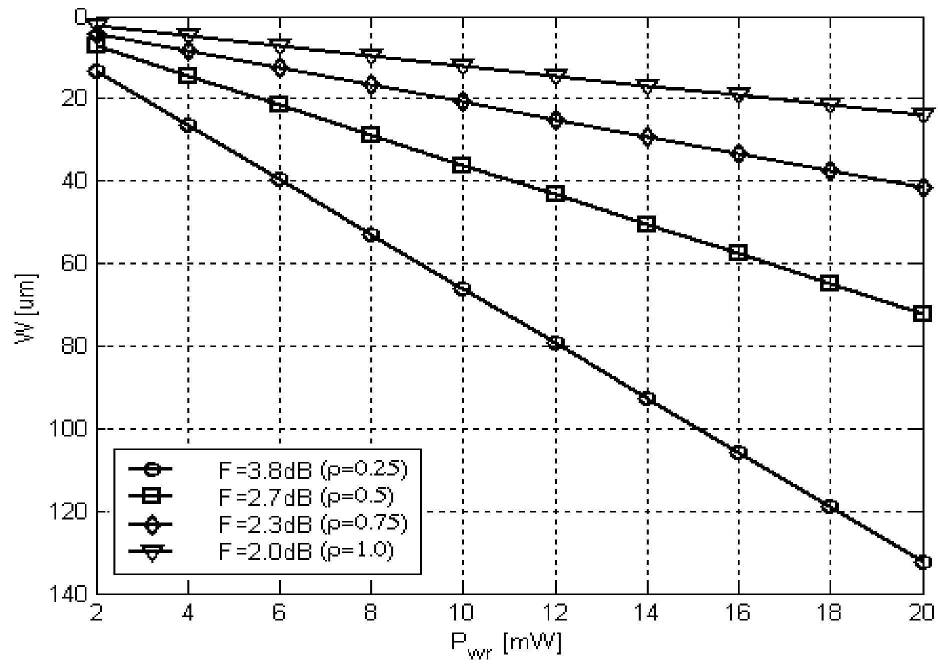


Fig. 2. Effect of χ on the noise performance for varing ρ values at 4GHz.

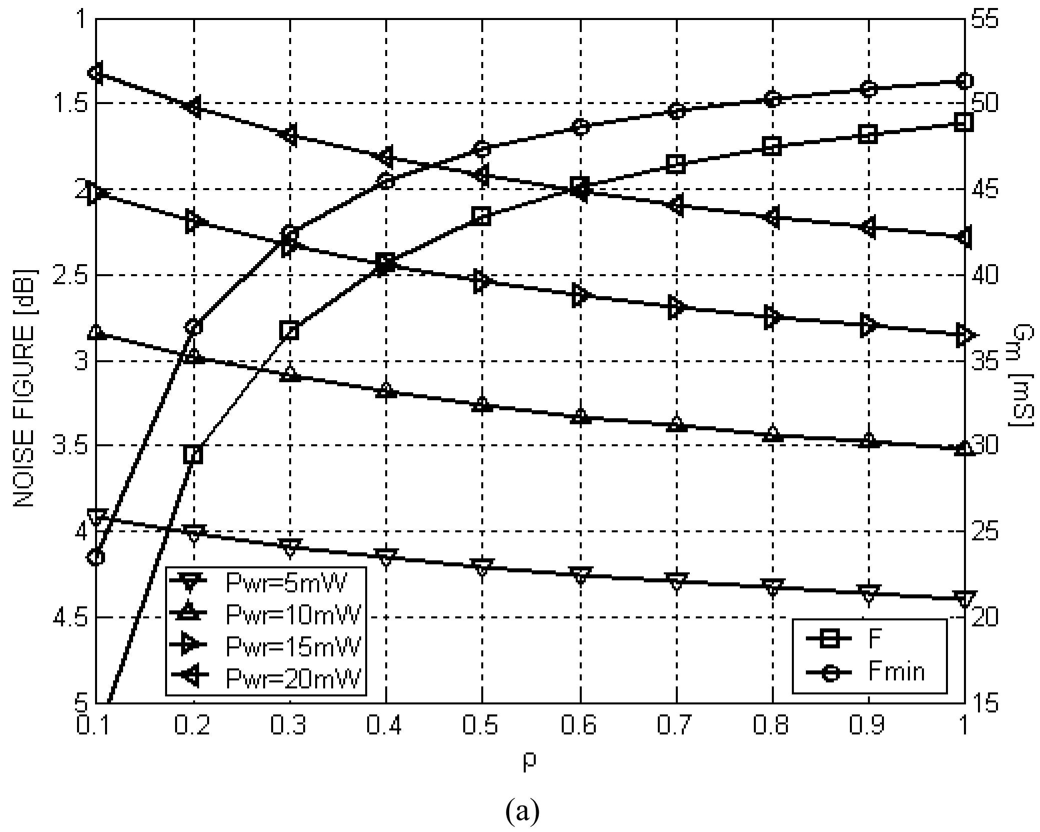


(a)

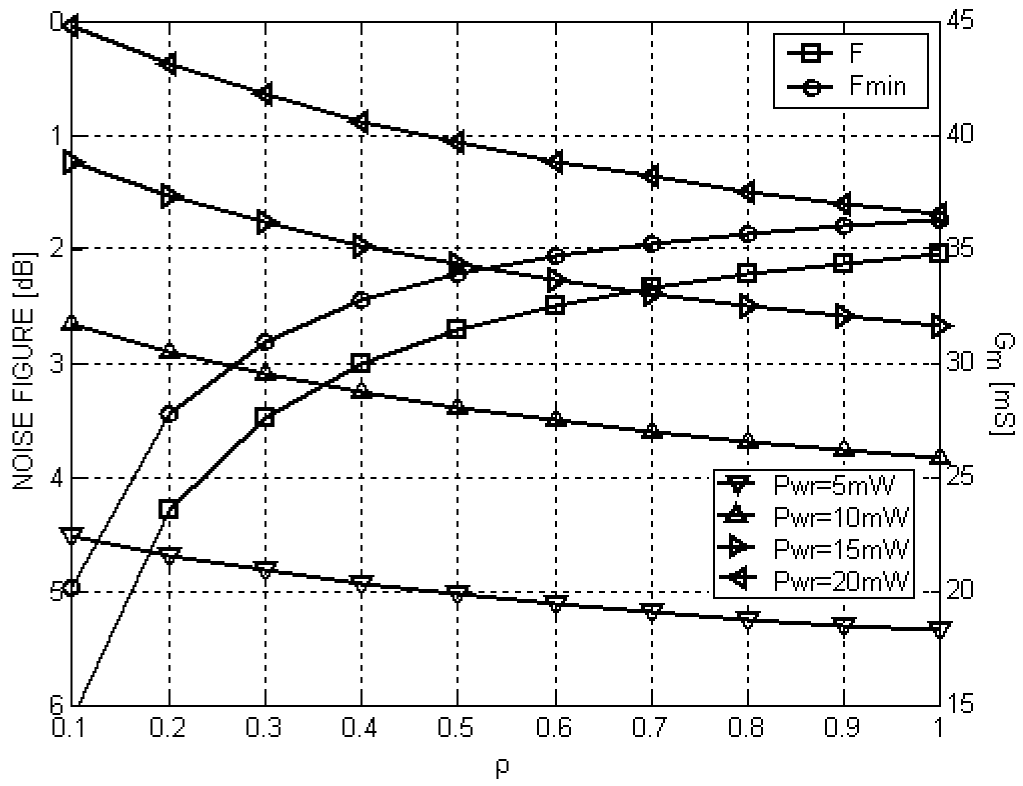


(b)

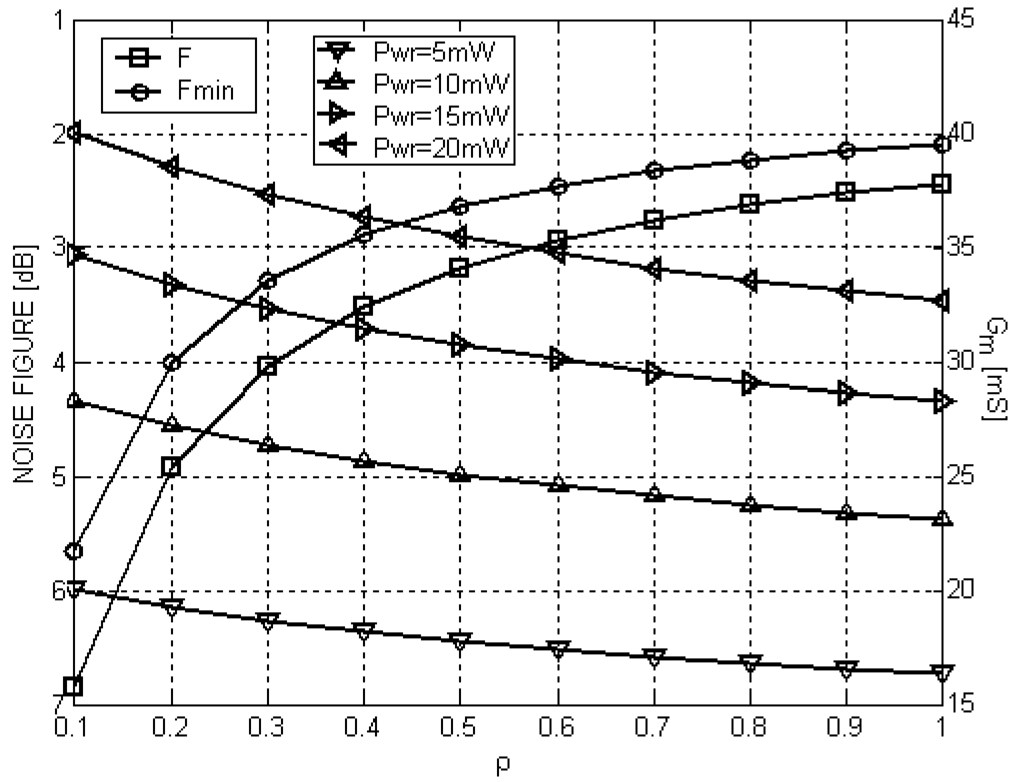
Fig. 3. Plots of (a) G_m vs. P_{wr} and (b) W vs. P_{wr} for different $F_{min,opt}$ (or ρ) values at 4GHz



(a)



(b)



(c)

Fig. 4. Plots of $F_{match,opt}$ and G_m subject to the power dissipation constraint (a) at 3GHz (b) at 4GHz (c) at 5GHz.

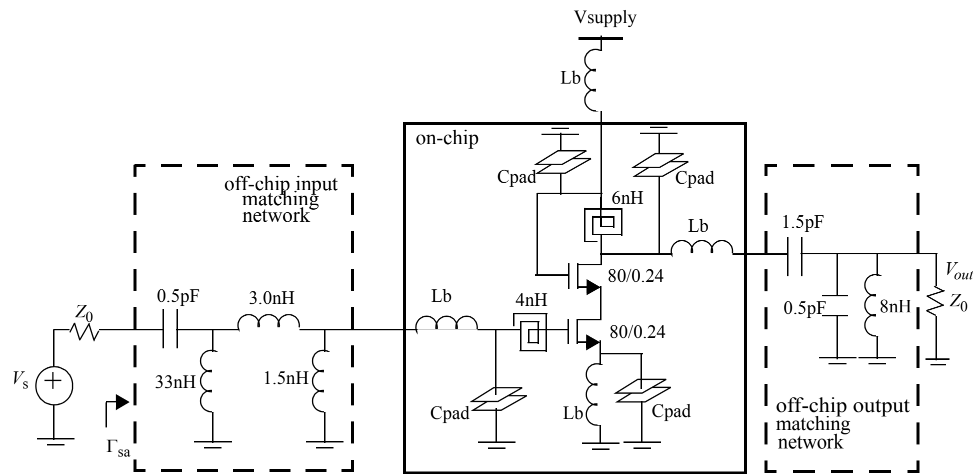


Fig. 5. Complete schmatic of the LNA testing setup (biasing not shown)

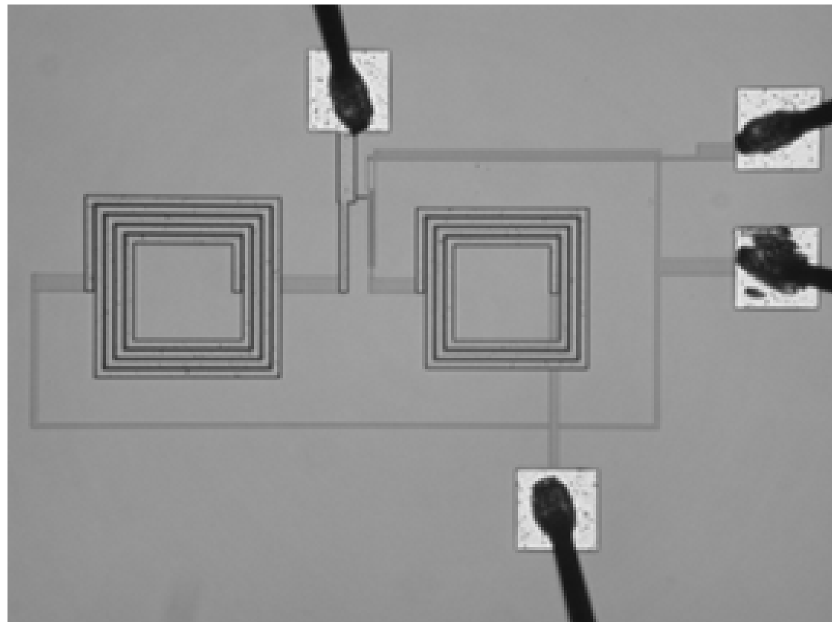


Fig. 6. Die photo of the LNA IC

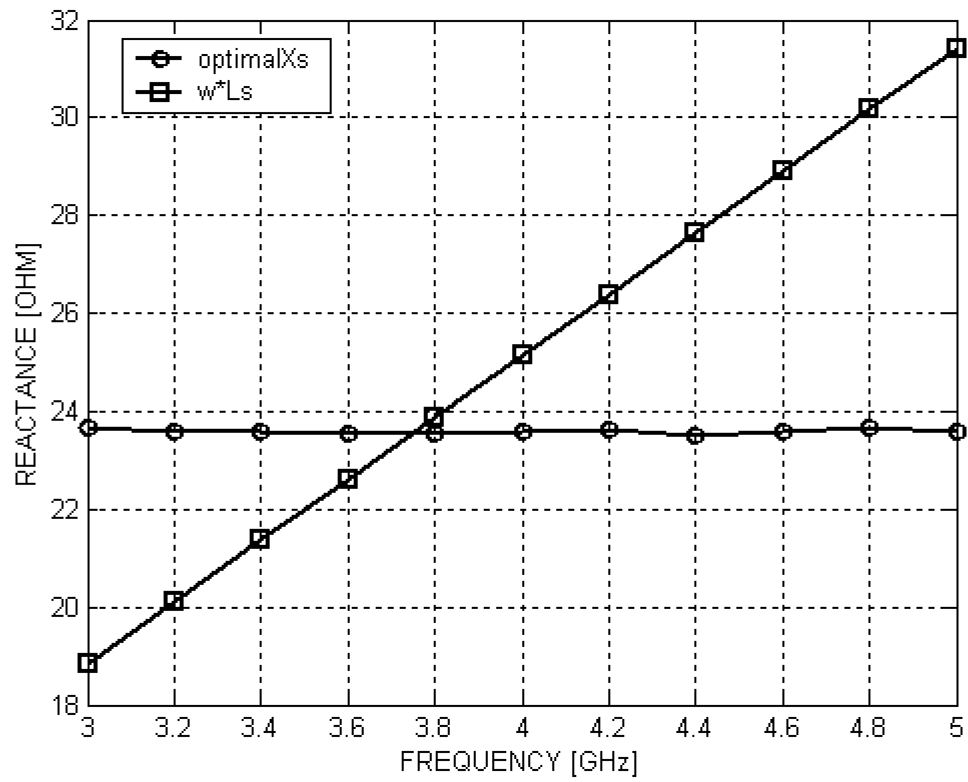


Fig. 7. Plots of the optimal source-degenration reactance and a single inductor of 1nH used to approximate the former.

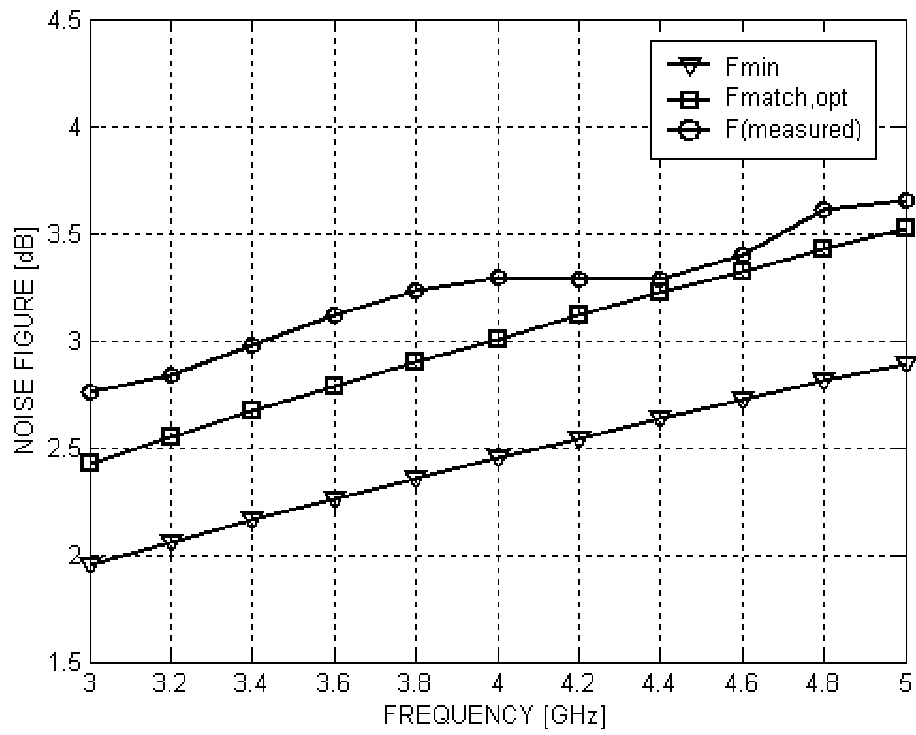


Fig. 8. Plot of the measured noise figure, as compared to the simulated $F_{match,opt}$ and F_{min}

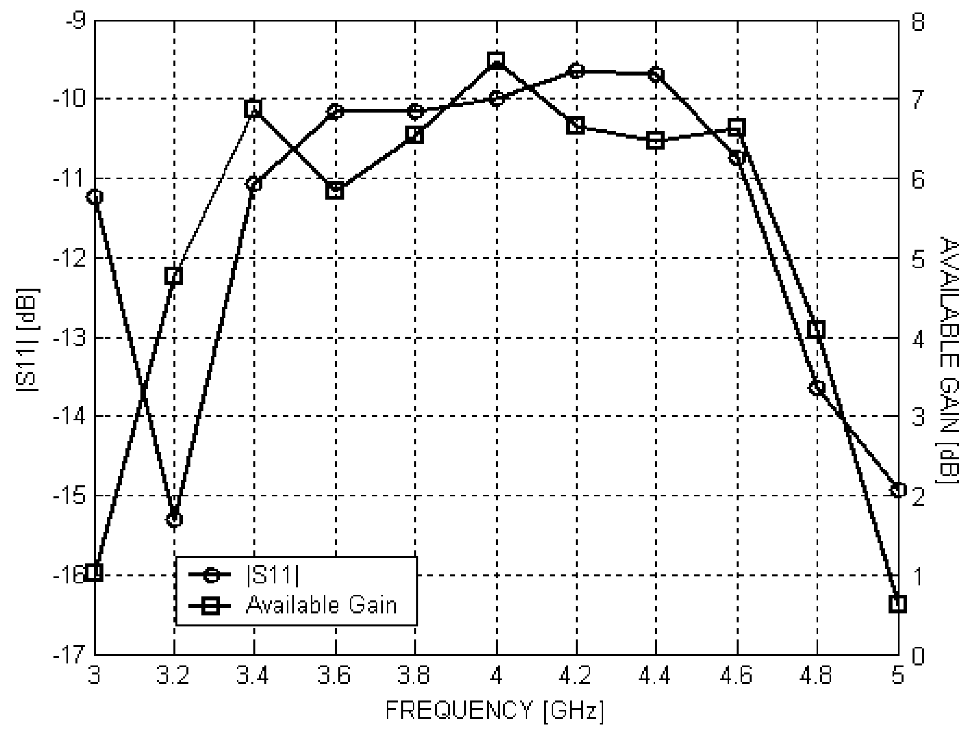


Fig. 9. Plots of the measured magnitude of S11 and available gain as a function of frequency

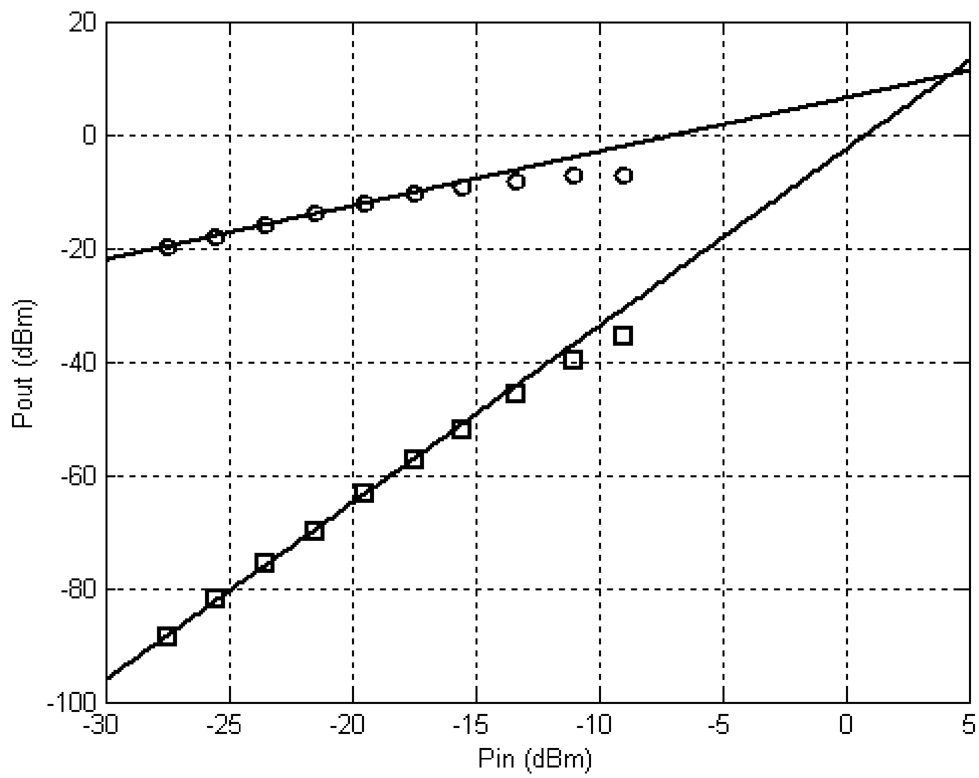


Fig. 10. Plots of the measured IIP3.