MURI 2002 Status

Bob Brodersen, David Tse, Ian O’Donnell, Mike Chen, Stanley Wang
Berkeley Wireless Research Center
Univ. of California, Berkeley
Project Areas

- Integration of UWB transceiver in CMOS
  - System simulations
  - Complete transceiver design
    - Antenna – LNA – baseband gain – Pulser
    - A/D
    - Digital baseband
- Realtime simulation of UWB systems
  - BEE FPGA array
  - UWB frontend
Flexible CMOS UWB Transceiver

- Our goal is to tape-out a single-chip UWB impulse transceiver by the end of the summer.
- This chip will have both the digital RX and control plus analog RX+TX blocks.
Flexibility for UWB system design exploration

- Different antennas (with impedance matching to the LNA)
- Variable transmit power
- Variable pulse rates
- Digital back-end will contain a programmable pulse-matched filter
- Adjustable data recovery/synchronization blocks
- Independent synchronization and data PN sequences
- I/O to send the A/D data directly to an external digital backend (i.e. BEE) for more sophisticated signal processing.
UWB Transceiver Prototype

Goal: Tape-out Single-Chip Transceiver by end of Summer
Desirable Functionality:
- Adjustable Slew Rate and Width
- Variable Magnitude Drive (I or V)
- Ability to Drive High or Low Impedance
- Digitally Programmable
- PAM (Binary Antipodal), and PPM (2 to 4 Steps)

Implementation:
- Differential Drive for PAM
- Multiplex DLL Clock Phases to Control Width and for PPM
- May Build Two Drivers and Selectively Connect/Enable for Experimentation
Pulse Reception

Parallel Sampling of Window of Time

Three Clocking Timescales:

- $T_{\text{SAMPLE}}$ (<ns)
- $T_{\text{WINDOW}}$ (~10’s ns)
- $T_{\text{PULSE\_REP}}$ (~100’s ns)
Antenna-LNA Co-design
UWB Antenna

- Requirements of UWB antennas for our applications
  - Broadband
  - Small size
  - Omni-directional
- Antennas meeting the above specifications do exist, e.g. loop antennas are very good candidates. Large Current Radiator (LCR) is one of them.
- Use EM simulator to characterize the antennas
- How about the interface?
  - Deem the antenna as a filter and then co-design antenna and circuits
Simulation in EM simulator

- Define the geometry & source
- Derives input voltage/current, input impedance, near/far zone transient fields, s-parameters, animation of the currents/fields/power flow, etc..
Equivalent Circuits for UWB Antennas

- Derive input impedance by simulations (UMass)
- Voltage-drive antenna will be capacitor-dominant while current-drive antenna will be inductor-dominant

![6cm Dipole Antenna Input Impedance](image)
Dipole/Monopole Antenna Model

- Compare the far-zone E-fields and the voltage across the radiation resistors of 4cm and 10cm dipole antennas
- Stimulated by a pulse with 50ohm source resistance
Flexible Antenna Driver

- Put the antenna circuit model into circuit simulator to design the driver
- H-bridge configuration
- Put them in parallel to make the driver flexible
Antenna/LNA Co-design

• Impedance of the Rx antenna seen by LNA is the same as that of the Tx antenna
• Optimize LNA by putting the antenna model in front
• Usually voltage-drive RX antennas prefer large $Z_{LNA}$ and current-drive antennas prefer small $Z_{LNA}$
Example: Monopole Rx Antennas

- 2cm monopole antenna with different loading
- Larger $\text{Z}_{\text{LNA}}$ gives higher LNA input voltage
- Mismatch due to scattering and near-zone field
- The relative magnitudes are close
Driver Circuit Simulation

- 1ns rise/fall-time input pulse
- Gaussian-derivative-shape waveform of the radiated E-field
- Imperfection of the waveforms due to nonlinearity of the driver and coupling between internal nodes
Driver Circuit Schematic

- Inverter chain sharpens the edge of the input signal
- Pre-driver NAND/NOR circuits skew the signals
  - Enable/Disable the driver
  - Avoid short-circuit current
  - Make the pulse radiated more balanced
Driver Circuit Layout

- STMicroelectronics 0.13um CMOS process
- Chip area: 0.49mm$^2$
- 1.2V Vdd
- 2 drivers with enables → Can either drive a monopole or dipole
- Each driver with 16 levels of driving capabilities
CMOS Analog Frontend
Timing generation

For Lower Power: Base System Clock on $T_{\text{WINDOW}}$

$T_{\text{SAMPLE}}$ Derived from DLL

$T_{\text{PULSE\_REP}} = \frac{T_{\text{WINDOW}}}{N}$
Oscillator Accuracy

Frequency Mismatch Causes Drift

Time to Slide One Sample Over One Received Bit; Given Mismatch, Pulse (Chip) Repetition Rate, and Length of PN Sequence.

\[ \frac{\Delta f}{f} \approx \frac{1}{2} \left( \frac{T_{\text{SAMPLE}}}{N_{\text{PN}} \cdot T_{\text{PULSE \_ REP}}} \right) \]

\[ f = \frac{(f_{\text{TX}} + f_{\text{RX}})}{2} ; \Delta f = (f_{\text{TX}} - f_{\text{RX}}) \]

\[ \begin{array}{c|c|c}
T_{\text{SAMPLE}} & 0.5\text{ns} \\
T_{\text{PULSE \_ REP}} & 100\text{ns} \\
N_{\text{PN}} & 1024 \\
T_{\text{WINDOW}} & 10\text{ns} \\
\hline
\Delta f/f & 2.4 \text{ PPM}
\end{array} \]
Oscillator Jitter

Phase Noise Bound:

Maximum Allowable Phase Noise for $\sigma_{\Delta T} = 100\text{ps}$ (per Oscillator) Over the Reception of One Bit.

\[
L\left\{\frac{\Delta w}{w}\right\} = \left(\frac{\sigma_{\Delta T}^2}{(\Delta w / w)^2 \Delta T}\right)
\]

<table>
<thead>
<tr>
<th>$T_{\text{SAMPLE}}$</th>
<th>0.5ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{\text{PULSE_REP}}$</td>
<td>100ns</td>
</tr>
<tr>
<td>$N_{\text{PN}}$</td>
<td>1024</td>
</tr>
<tr>
<td>$T_{\text{WINDOW}}$</td>
<td>10ns</td>
</tr>
</tbody>
</table>

$L\{100\text{kHz}/100\text{MHz}\} = -100\text{dBc}$

$(\sigma_{\Delta T} = 100\text{ps})$
RX: Clock Generation

EXTERNAL CRYSTAL

OSCILLATOR

PHASE DETECTOR

CHARGE PUMP & LOOP FILTER

VARIABLE DELAY LINE

BUFFER

$T_{\text{SAMPLE}} = \frac{T_{\text{WINDOW}}}{N}$

$T_{\text{WINDOW}}$
RX: LNA

**Desirable Functionality:**

- Gain ~ 10 V/V over ~ 1GHz BW
- Noise Figure < 10dB (Not Critical In an Interference Dominated Environment)
- Differential Input
- Handle Multiple Antennas (I.e. Current Loop and/or Dipole)
- Switch Bias On/Off within $T_{\text{WINDOW}}$
- Fast Overload Recovery (Track Full-Scale 1GHz Sinusoid)

**Implementation:**

May Build Two Amplifiers and Selectively Connect/Enable for Experimentation
Desirable Functionality:

- Minimum Gain = 1,000
- Partition Gain/Stages for Minimum Current Consumption
- Capacitive Coupling Between Stages (Null DC Offset)
- Switch Bias On/Off within $T_{\text{WINDOW}}$
- Fast Overload Recovery (Track Full-Scale 1GHz Sinusoid)
- Additionally Include Filtering for Frequencies $< 100\text{MHz}$, $> 1\text{GHz}$
- Last Stage Drives Sampling Switch Load (could be ~100’s fF)
RX: A/D Comparator requirement

1-Sigma $V_{OFFSET}$ for Fixed Tracking BW=1GHz

$V_{OFFSET}$ ~ 20mV (w/ No Explicit Cancellation) for $C_{SAMPLE} > 10fF$
Overview of UWB baseband
Specs for Baseband

- Pulse Repetition Rate: 1MHz to 100 MHz
- Maximum receivable Pulse ripple length \((N_{\text{ripple}} = N_{\text{pulse}} + N_{\text{spread}})\): < 64ns (128 samples)
- Sampling rate: 2 GHz
- PN spread ranges from 1 to 1024 chips
Baseband Overview

PMF

PN Gen

Coef

PN correlator 1

PN correlator 2

PN correlator 128

Peak Det

Correlation_Block

Data PN Correlator

Data Recover (soft/hard)

Control logic

Symbol Strobe

CLKA

CLKC

fchip

8

S / P

256

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CLKC

fchip

8

S / P

256

Berkeley Wireless Research Center
Operation Modes

- **Acquisition mode:**
  Receiver tries to lock the signal with a certain PN phase. The implementation uses a mixed mode of parallel and serial search, depends on the tradeoffs between hardware and acquisition time.

- **Tracking mode:**
  Track the sampling time error caused by the changing channel, sampling clock offset between transmitter and receiver. If the signal is moving toward the boundary of sampling window, it will feedback a control signal to front end to shift the sampling window. And we take the maximum signal to do data recovery.
Acquisition mode

- Searching for the peak at the output of correlators

From PN generator

ADC

PN Correlator 1

PN Correlator 2

PN Correlator 128

Threshold
Tracking mode

[Diagram showing PN correlators and data recovery process]

Data Recovery
1. Hard decision (symbol detection).
2. Soft Sequence detection, such as Viterbi decoding.

Feedback to front end
Control logic

- A read clock to fetch the PN phase and a programmable PN length is needed.
- Strobe_phase signal is used to define the symbol boundary after entering tracking mode.
- A enable/disable control bus is needed for gated clock in PN correlators for power saving purpose.
Simulink Implementation

S/P
PMF
fsym
PN Generator
PN correlators
S/P
PN Generator
ASIC Design Decisions
Processing Gain

• For an Input Eb/No = -11dB 1024 chips is more than enough. (1) Acquisition mode, ~400 chips is enough for suppressing the acquisition error below 1e-3.

<table>
<thead>
<tr>
<th>Chips</th>
<th>Prob. of Miss lock</th>
<th>Prob. of False alarm</th>
<th>EbNo @ output</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>0.0037</td>
<td>0.0041</td>
<td>14.4245 dB</td>
</tr>
<tr>
<td>400</td>
<td>0.86e-3</td>
<td>1.3e-3</td>
<td>15.6643 dB</td>
</tr>
</tbody>
</table>

(2) Data recovery mode, ~100 chips could achieve an uncoded bit error rate of 1e-3.

<table>
<thead>
<tr>
<th>Chips</th>
<th>BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0.1663</td>
</tr>
<tr>
<td>100</td>
<td>1.1e-3</td>
</tr>
<tr>
<td>200</td>
<td>2e-5</td>
</tr>
</tbody>
</table>
Parallel vs. Serial Acquisition

- Assume the worst case using 1024 PN chips, while pulse rate is equal to 100 ns. We need to choose somewhere in between.

(1) Acquisition Time
- Fully Parallel: 0.1 ms
- Serial: 0.1 sec

(2) Area Cost
- Fully Parallel: 500 mm$^2$
- Serial: 5.8 mm$^2$
Partial Acquisition

- Once number of parallel search phases are above 10, product of area cost and acquisition time begins to saturate. Not beneficial to increase more search phases.
- No. of searching phases is chosen to be 11 in the design.
<table>
<thead>
<tr>
<th>Block</th>
<th>Area (mm²)</th>
<th>Power (Acq)</th>
<th>Power(Track)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse Matched Filter</td>
<td>4.95</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>(256 inputs, 128 outputs)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PN Generator</td>
<td>.23</td>
<td>N/A</td>
<td>1.14 mW</td>
</tr>
<tr>
<td>(max 1024 chips)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak detector Block</td>
<td>2.88</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>(128 inputs)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Recovery</td>
<td>.069</td>
<td>0</td>
<td>54.7 uW</td>
</tr>
<tr>
<td>(Track 3 samples)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Control Logic</td>
<td>&lt;.001</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>(state flow)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PN correlators</td>
<td>2.47</td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td>(contain 128 correlators)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td>10.6</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Area Distribution on Chip

- The biggest single block is PMF (Pulse Matched Filter), which is implemented in Carry-save adders.
- PN correlators and Peak detectors are proportional to the number of searching phases. The optimal point makes this area comparable to PMF.
BEE FPGA Array
What’s BEE?

- A real time hardware emulator built from 20 high-density Field Programmable Gate Arrays (FPGAs).
- Emulation capacity of 10 Million ASIC gate-equivalents per module, corresponding to 600 Billion operations (16-bit adds) per second.
- Realistic emulation speed 10 – 100 MHz
- 2400 external I/O for add-ons, like radios.
- Automated design flow from Simulink to FPGA emulation, integrated with the Chip-in-a-Day ASIC design flow.
Power Board PCB connected to BPU
Simulink - 5120 tap FIR design
5120 Tap FIR filter design (cont.)

80 MHz sample rate
.8 Teraops/sec
UWB Transceiver Frontend

Receiver
1.2 Gsamples/second, 7 bits

Transmitter
CMOS H-bridge

2 control bits (LVDS pairs) from the BEE

60-LVDS Pairs @ 155MHz to the BEE

VGA and PLL Control from the BEE
UWB Transceiver board

- Power Supply Regulators
  - +5V Analog
  - -5V Analog
  - +5V Digital
  - +3.3V Digital

- ADC
- PECL
- Delay1:20 PECL
- Clock Driver
- PLL
- LVDS Receivers
- 1:4 Deserializers
- Ref.
- LNA/VGA
- 4-pole Butterworth
- 68-pin HDSCSI connector
- PLL
- PECL
- 1:20 PECL
- Clock Driver
- 68-pin HDSCSI connector
- UWB Transceiver board
Status Summary

- First pass system design completed with full simulations
- Analog circuit design approximately 50% completed
- Digital baseband design completed, backend design beginning
- BEE FPGA fabricated and fully functional
- BEE UWB frontend designed