MURI 2002 Status

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Berkeley Wireless Research Center

Univ. of California, Berkeley

Project Areas

- Integration of UWB transceiver in CMOS
  - System simulations
  - Complete transceiver design
    - Antenna – LNA – baseband gain – Pulser
    - A/D
    - Digital baseband
- Realtime simulation of UWB systems
  - BEE FPGA array
  - UWB frontend

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Flexible CMOS UWB Transceiver

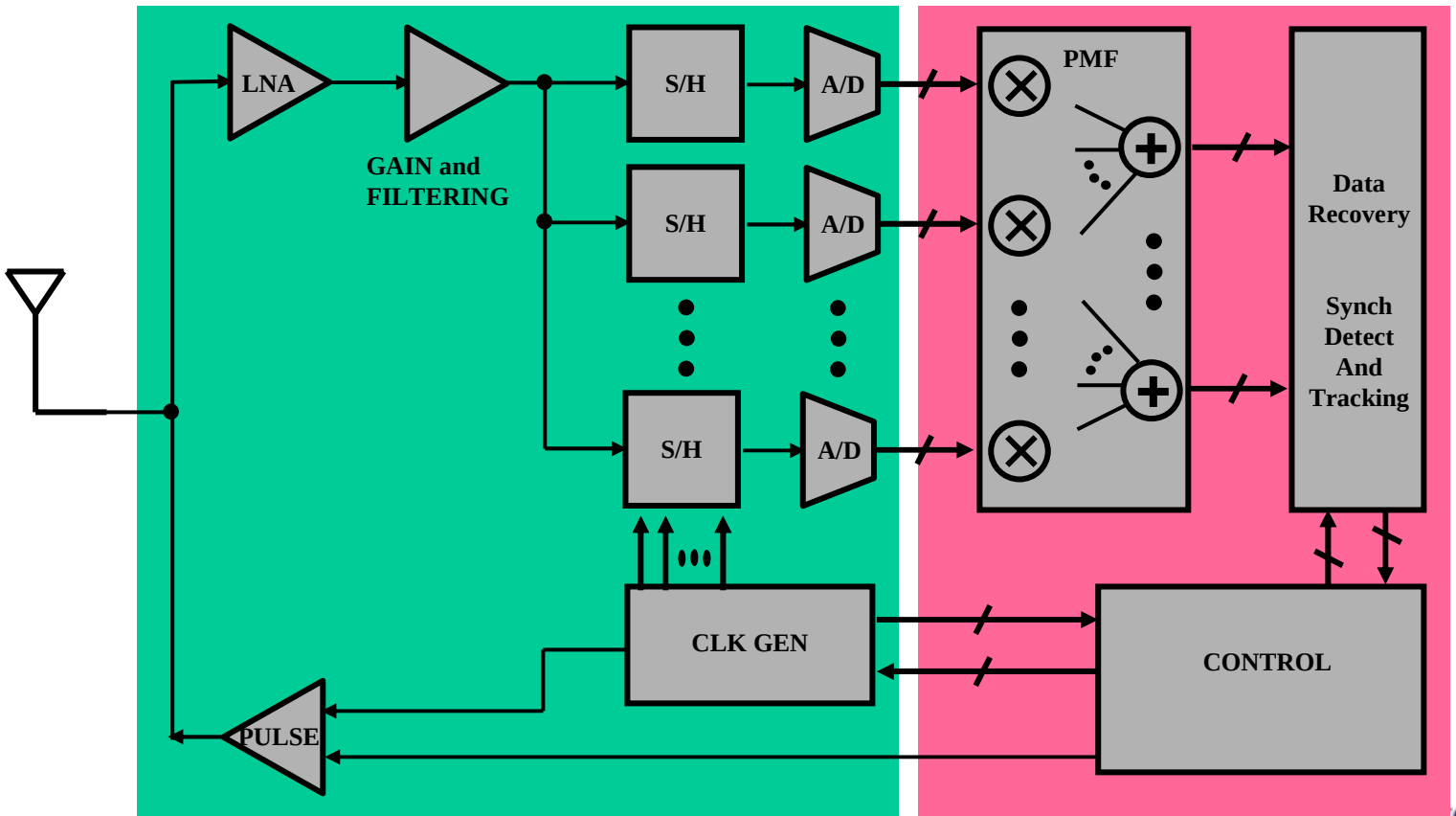
- Our goal is to tape-out a single-chip UWB impulse transceiver by the end of the summer.
- This chip will have both the digital RX and control plus analog RX+TX blocks.

Flexibility for UWB system design exploration

- Different antennas (with impedance matching to the LNA)
- Variable transmit power
- Variable pulse rates
- Digital back-end will contain a programmable pulse-matched filter
- Adjustable data recovery/synchronization blocks
- Independent synchronization and data PN sequences
- I/O to send the A/D data directly to an external digital backend (i.e. BEE) for more sophisticated signal processing.

UWB Transceiver Prototype

Goal: Tape-out Single-Chip Transceiver by end of Summer



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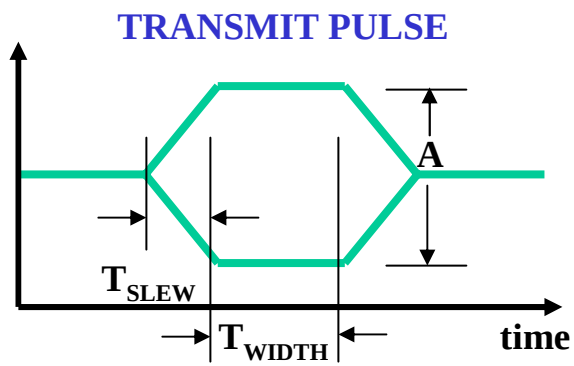
Pulse Transmitter

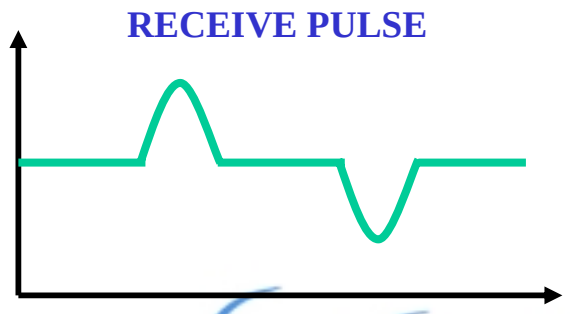
Desirable Functionality:

- Adjustable Slew Rate and Width
- Variable Magnitude Drive (I or V)
- Ability to Drive High or Low Impedance
- Digitally Programmable
- PAM (Binary Antipodal), and
  PPM (2 to 4 Steps)



Implementation:

Differential Drive for PAM
Multiplex DLL Clock Phases to Control
Width and for PPM
May Build Two Drivers and Selectively
Connect/Enable for Experimentation



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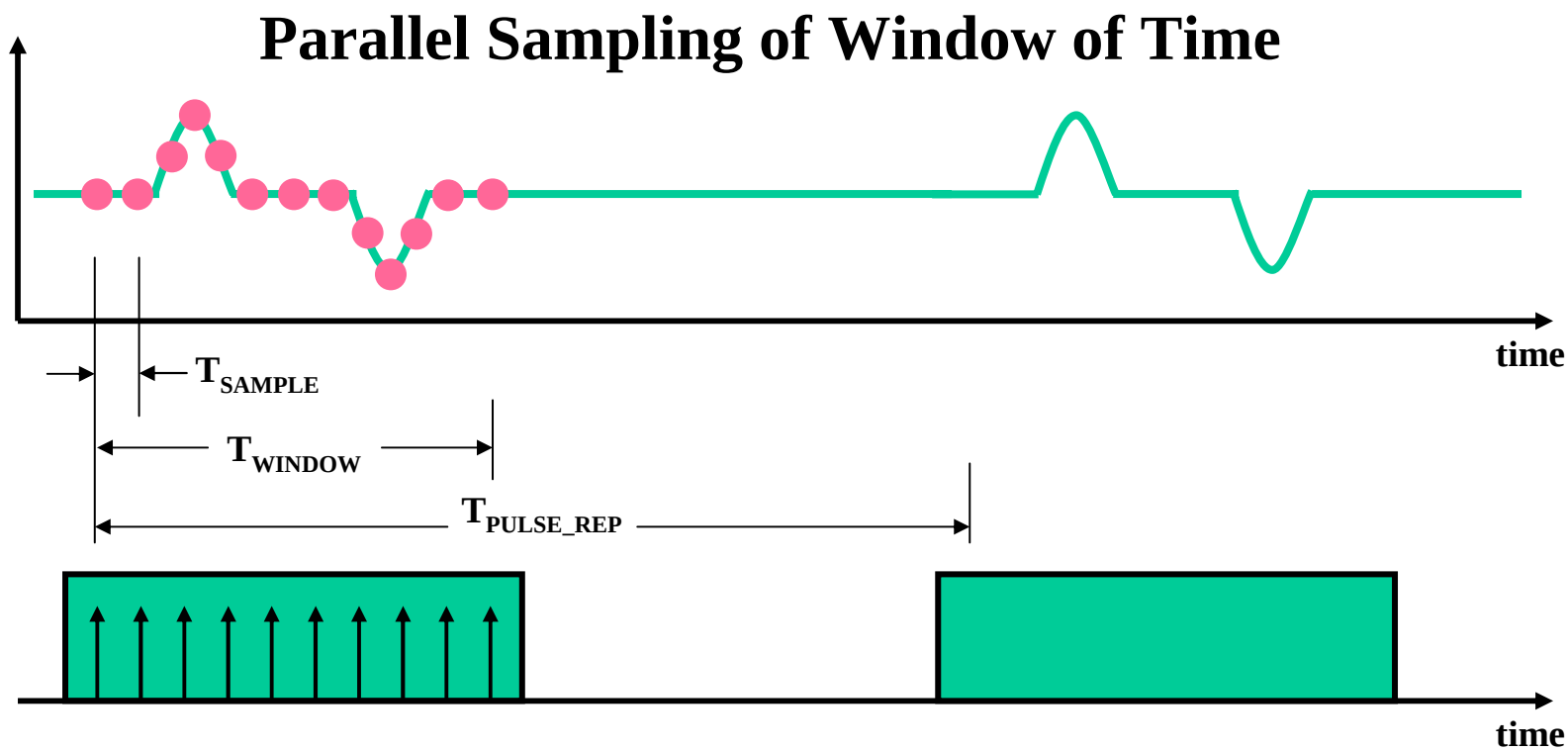
Pulse Reception



Three Clocking Timescales:

T_{SAMPLE} (<ns) T_{WINDOW} (~10's ns) T_{PULSE_REP} (~100's ns)

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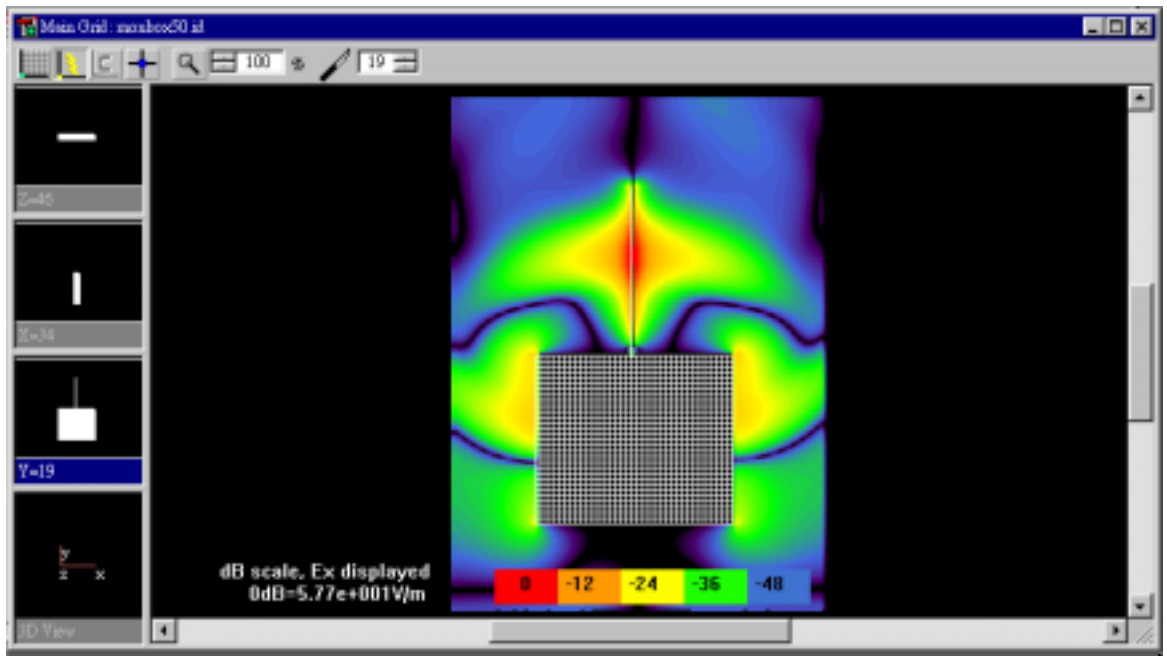
Antenna-LNA Co-design

UWB Antenna

- Requirements of UWB antennas for our applications
  - Broadband
  - Small size
  - Omni-directional
- Antennas meeting the above specifications do exist, e.g. loop antennas are very good candidates. Large Current Radiator(LCR) is one of them.
- Use EM simulator to characterize the antennas
- How about the interface?
  - Deem the antenna as a filter and then co-design antenna and circuits

Simulation in EM simulator

- Define the geometry & source
- Derives input voltage/current, input impedance, near/far zone transient fields, s-parameters, animation of the currents/fields/power flow, etc..



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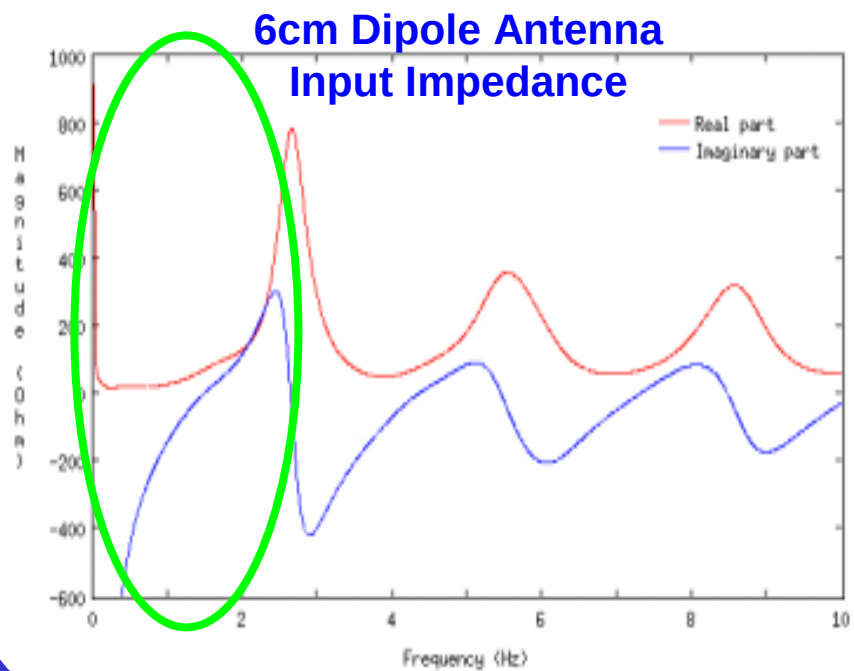
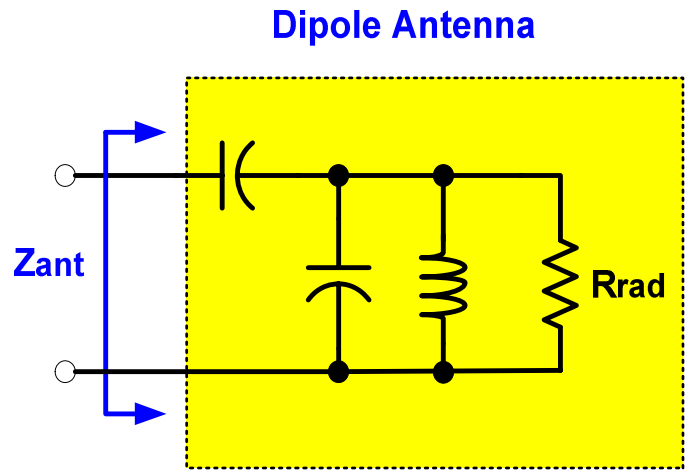
Equivalent Circuits for UWB Antennas

- Derive input impedance by simulations (UMass)
- Voltage-drive antenna will be capacitor-dominant while current-drive antenna will be inductor-dominant





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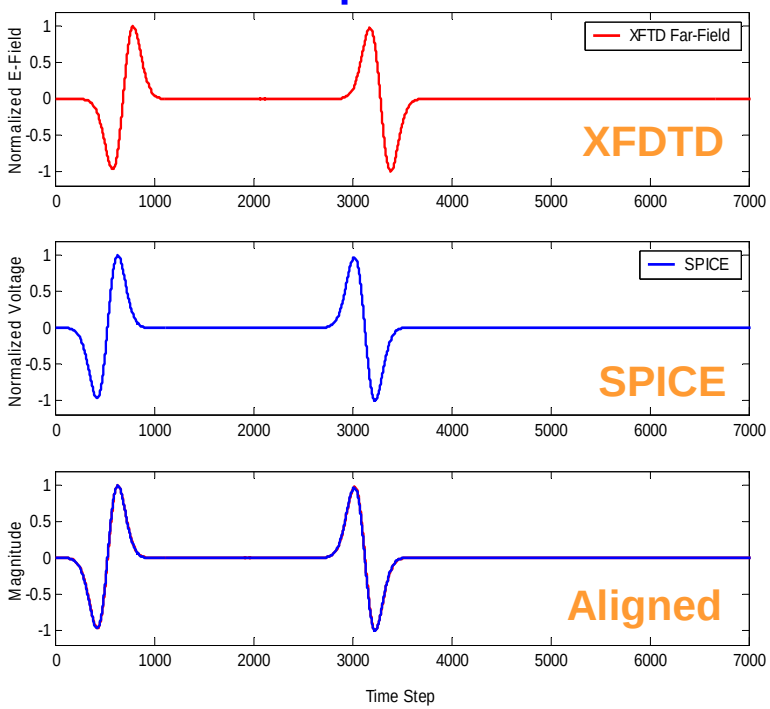
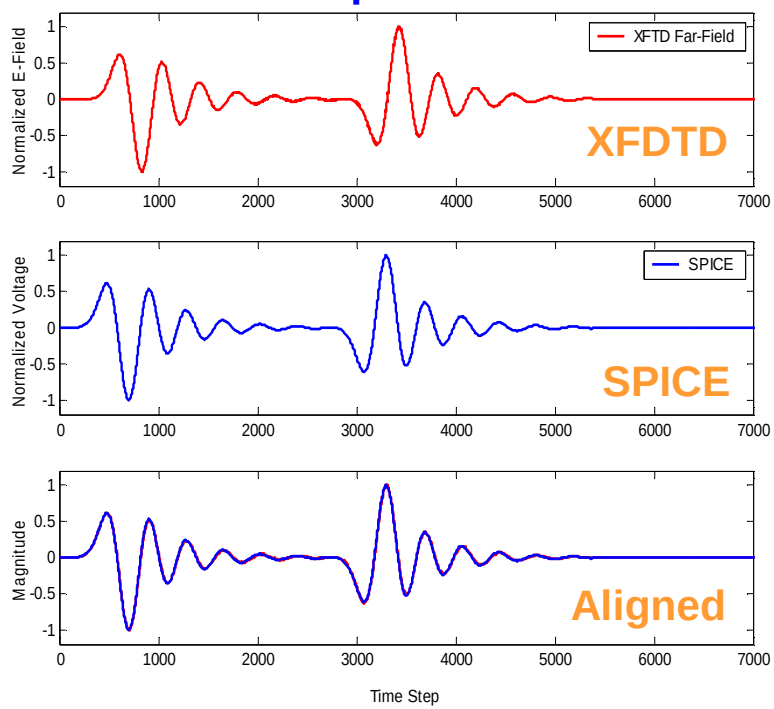
Dipole/Monopole Antenna Model

- Compare the far-zone E-fields and the voltage across the radiation resistors of 4cm and 10cm dipole antennas
- Stimulated by a pulse with 50ohm source resistance

4cm Dipole Antenna



10cm Dipole Antenna



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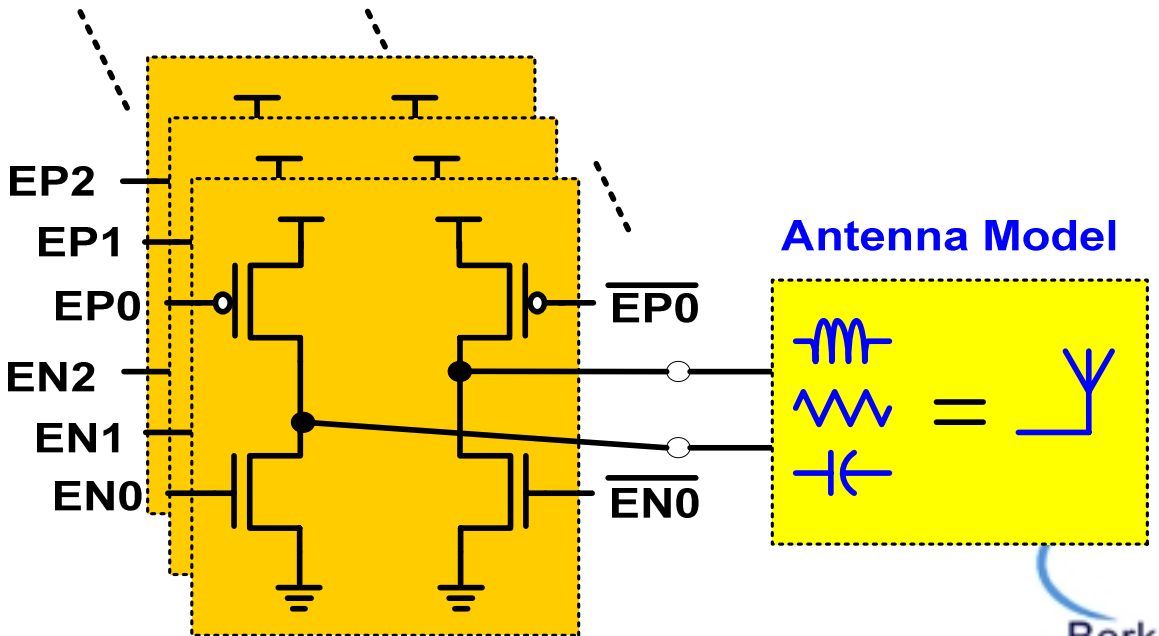
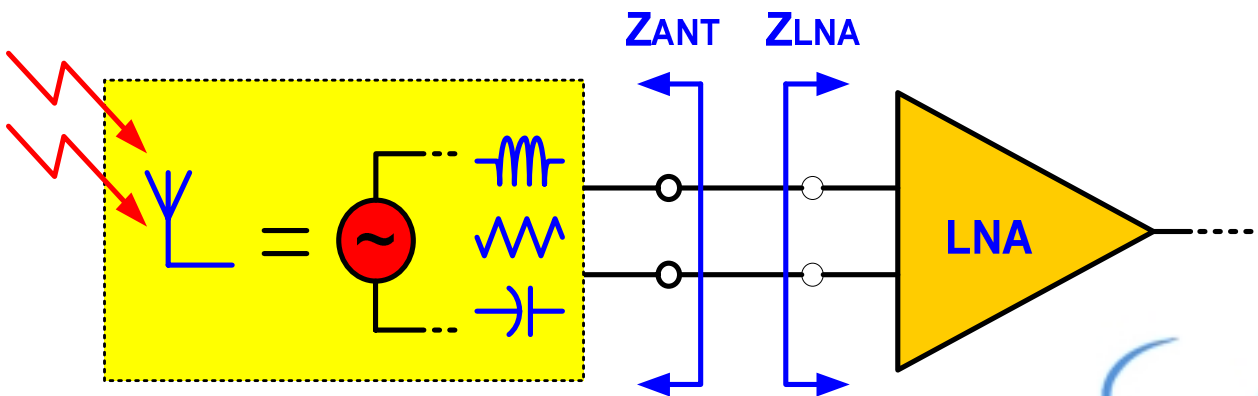
Flexible Antenna Driver

- Put the antenna circuit model into circuit simulator to design the driver
- H-bridge configuration
- Put them in parallel to make the driver flexible



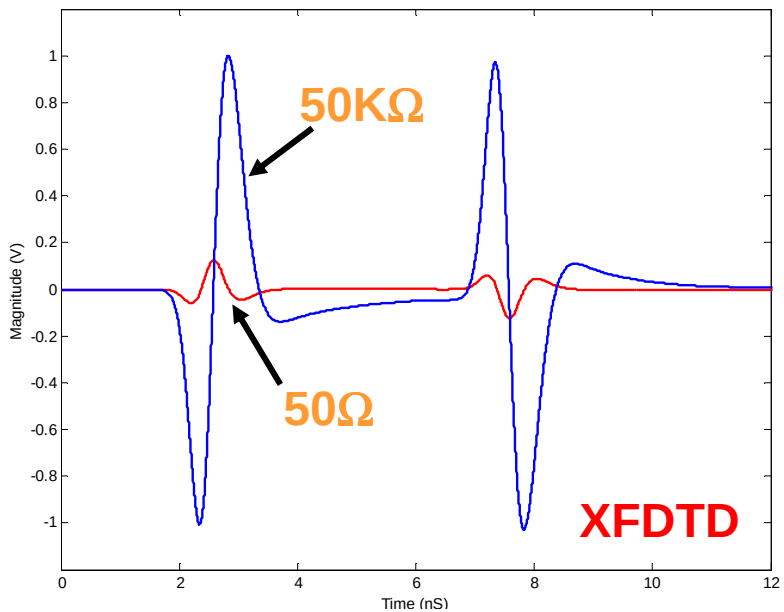
Antenna/LNA Co-design

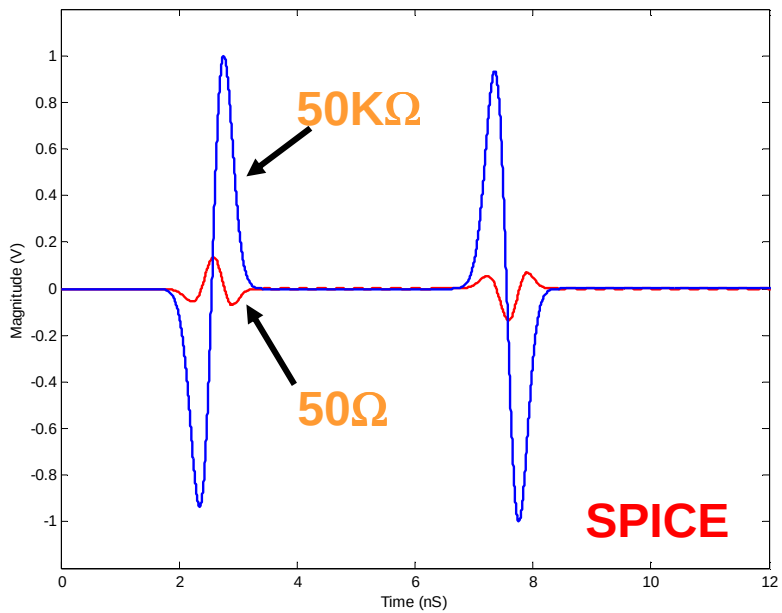
- Impedance of the Rx antenna seen by LNA is the same as that of the Tx antenna
- Optimize LNA by putting the antenna model in front
- Usually voltage-drive RX antennas prefer large Z_{LNA} and current-drive antennas prefer small Z_{LNA}



Example: Monopole Rx Antennas

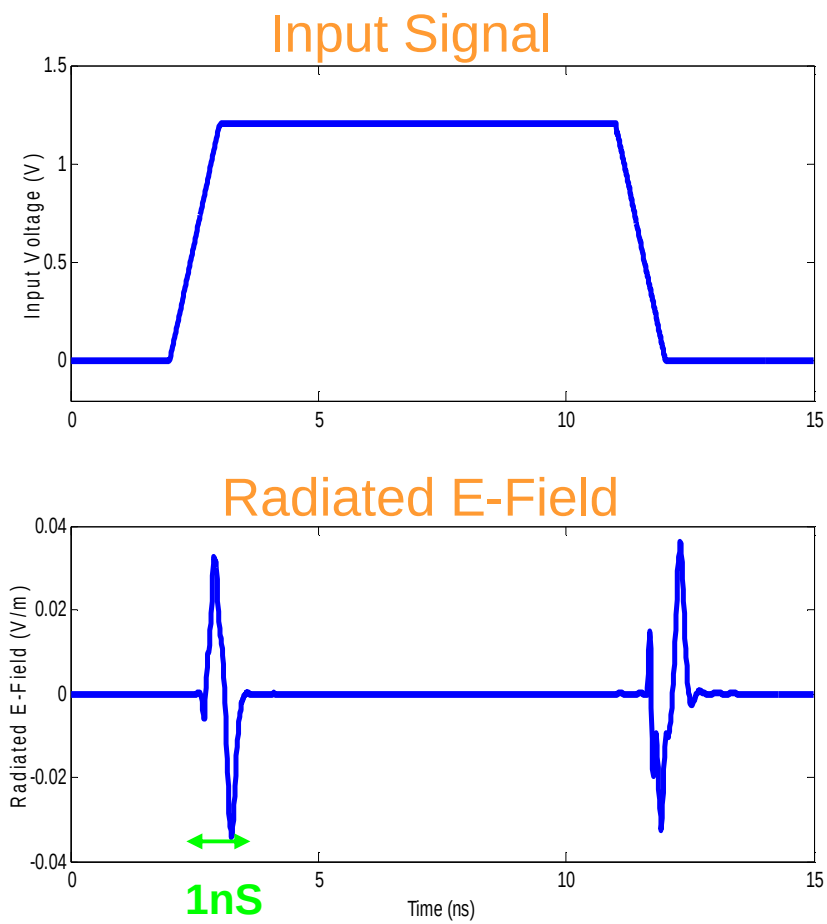
- 2cm monopole antenna with different loading
- Larger Z_{LNA} gives higher LNA input voltage
- Mismatch due to scattering and near-zone field
- The relative magnitudes are close





Driver Circuit Simulation

- 1ns rise/fall-time input pulse
- Gaussian-derivative-shape waveform of the radiated E-field
- Imperfection of the waveforms due to nonlinearity of the driver and coupling between internal nodes



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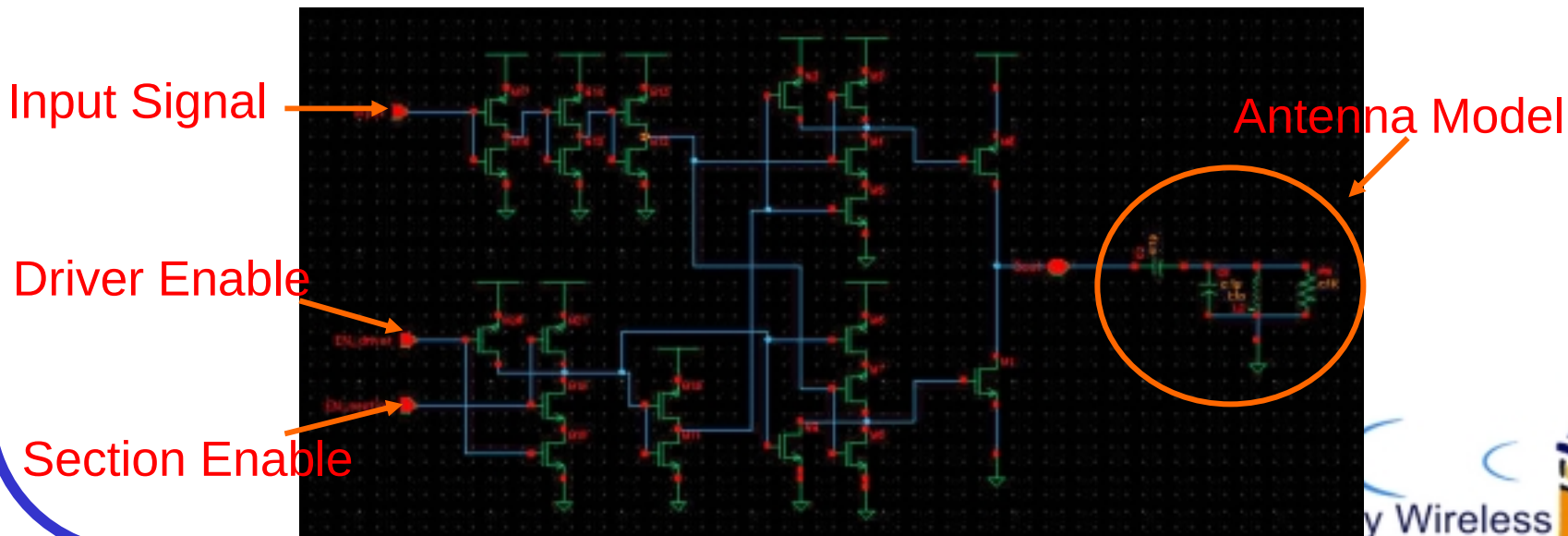
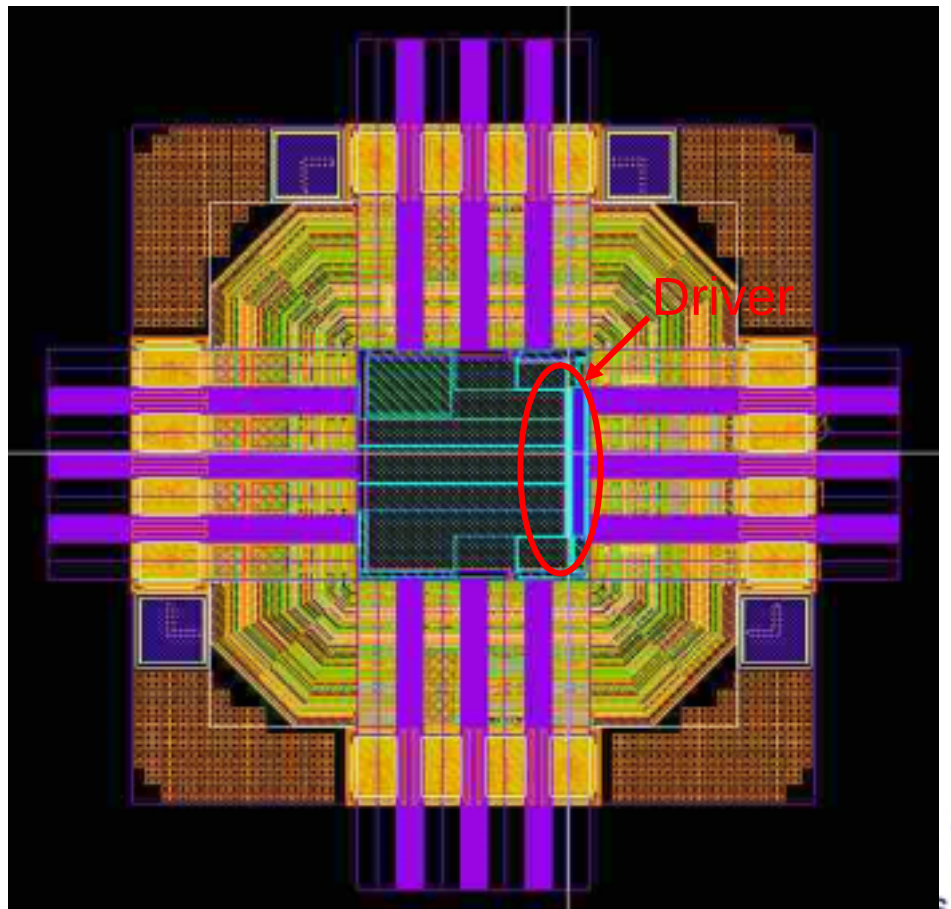
Driver Circuit Schematic

- Inverter chain sharpens the edge of the input signal
- Pre-driver NAND/NOR circuits skew the signals
  - Enable/Disable the driver
  - Avoid short-circuit current
  - Make the pulse radiated more balanced



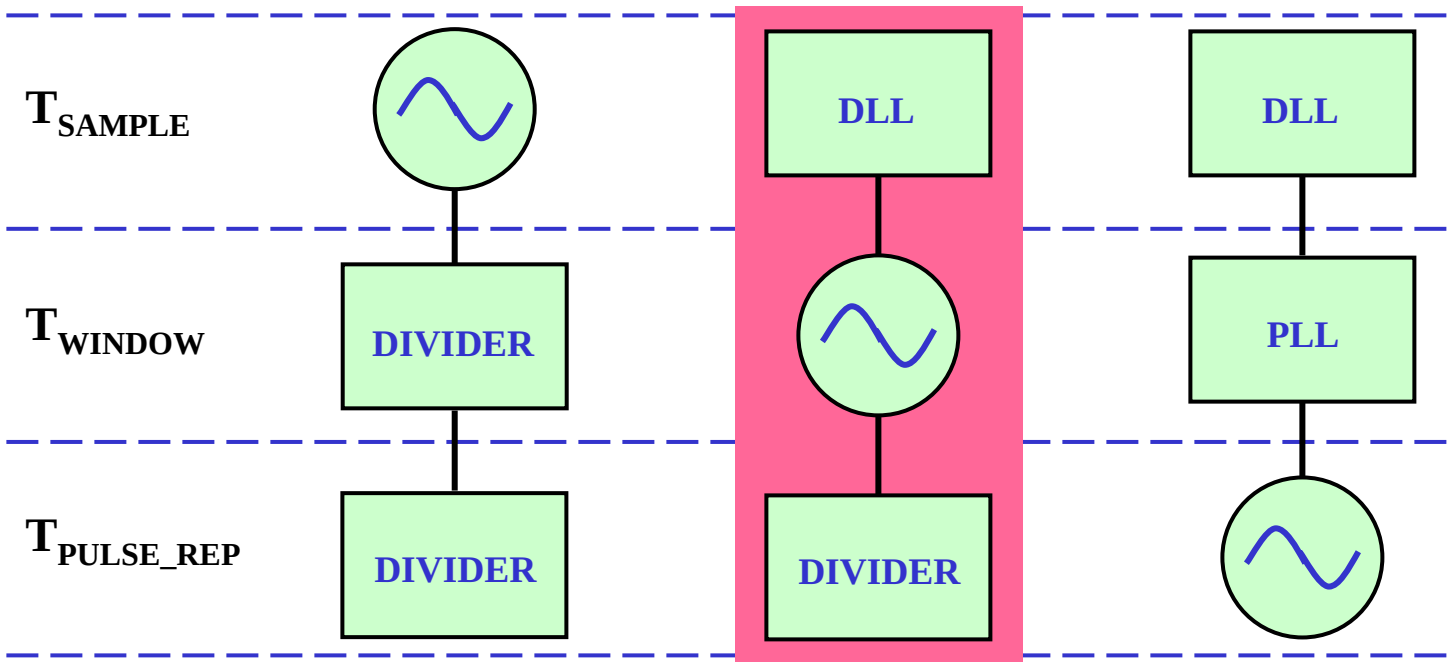
Driver Circuit Layout

- STMicroelectronics 0.13um CMOS process
- Chip area: 0.49mm^2
- 1.2V Vdd
- 2 drivers with enables → Can either drive a monopole or dipole
- Each driver with 16 levels of driving capabilities



CMOS Analog Frontend

Timing generation



For Lower Power: Base System Clock on T_{WINDOW}

T_{SAMPLE} Derived from DLL

$T_{PULSE\_REP} = T_{WINDOW} / N$

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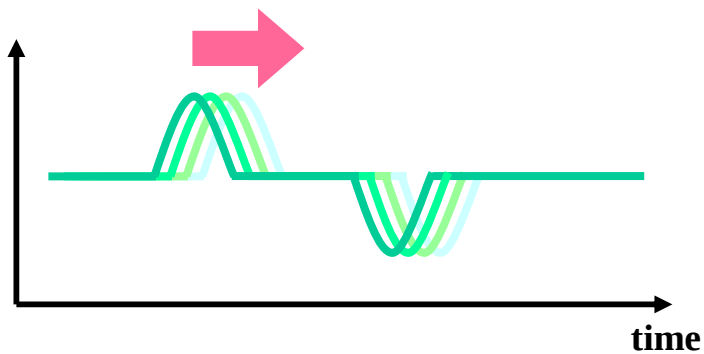
Oscillator Accuracy

Frequency Mismatch Causes Drift

Time to Slide One Sample Over One Received Bit; Given Mismatch, Pulse (Chip) Repetition Rate, and Length of PN Sequence.

$$\frac{\Delta f}{f} \approx \frac{1}{2}\left(\frac{T_{SAMPLE}}{N_{PN} \cdot T_{PULSE\_REP}}\right)$$

$f = (f_{TX} + f_{RX})/2$; $\Delta f = (f_{TX} - f_{RX})$



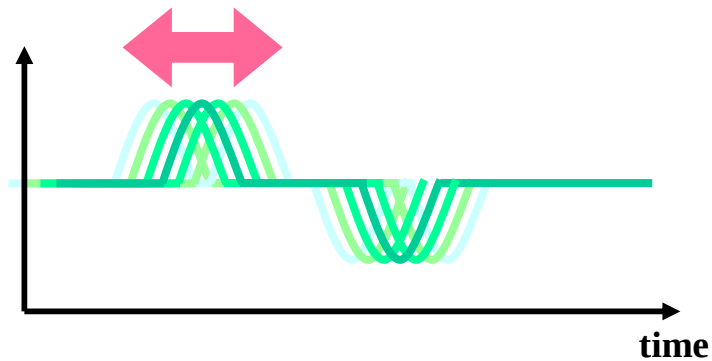
T_{SAMPLE} = 0.5ns T_{PULSE_REP} = 100ns N_{PN} = 1024 T_{WINDOW} = 10ns	$\Delta f/f$ = 2.4 PPM

Oscillator Jitter

Phase Noise Bound:

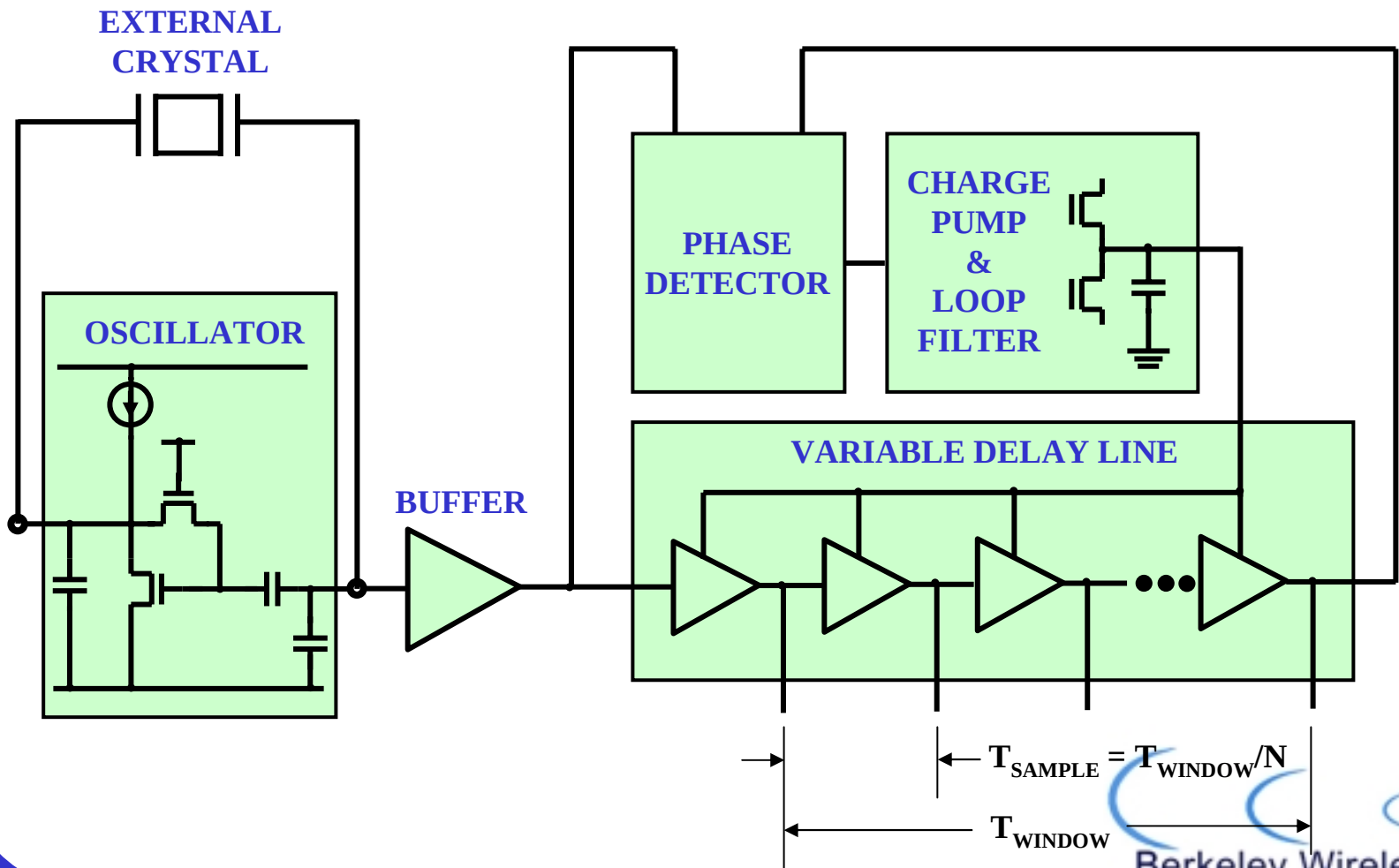
Maximum Allowable Phase Noise for $\sigma_{\Delta T}$ = 100ps (per Oscillator) Over the Reception of One Bit.

$$L\{\frac{\Delta w}{w}\} = \left(\frac{\sigma_{\Delta T}^2}{(\Delta w / w)^2 \Delta T} \right)$$



T_{SAMPLE} = 0.5ns T_{PULSE_REP} = 100ns N_{PN} = 1024 T_{WINDOW} = 10ns	L{100kHz/100MHz} = -100dBc ($\sigma_{\Delta T}$ = 100ps)

RX: Clock Generation



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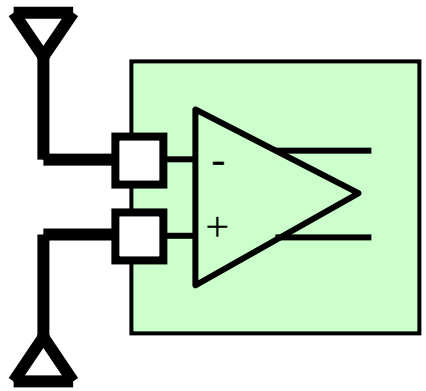
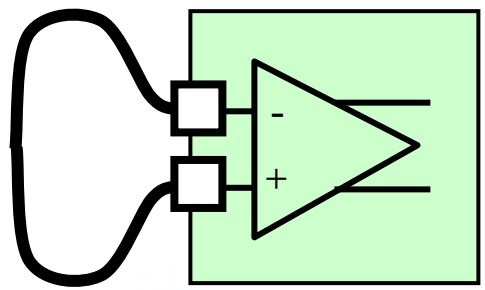
RX: LNA

Desirable Functionality:

- Gain ~ 10 V/V over ~ 1GHz BW
- Noise Figure < 10dB (Not Critical In an Interference Dominated Environment)
- Differential Input
- Handle Multiple Antennas (I.e. Current Loop and/or Dipole)
- Switch Bias On/Off within T_{WINDOW}
- Fast Overload Recovery (Track Full-Scale 1GHz Sinusoid)





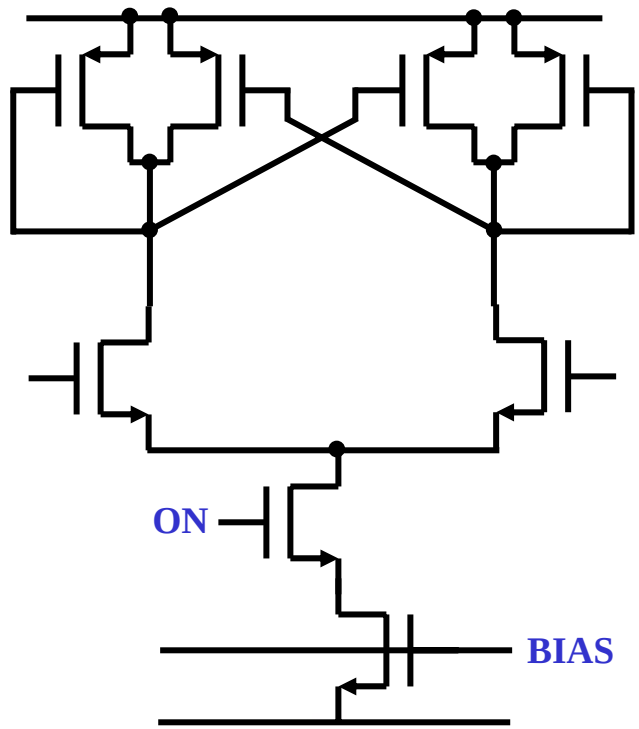
Implementation:

May Build Two Amplifiers and Selectively Connect/Enable for Experimentation

RX: Gain + Filtering

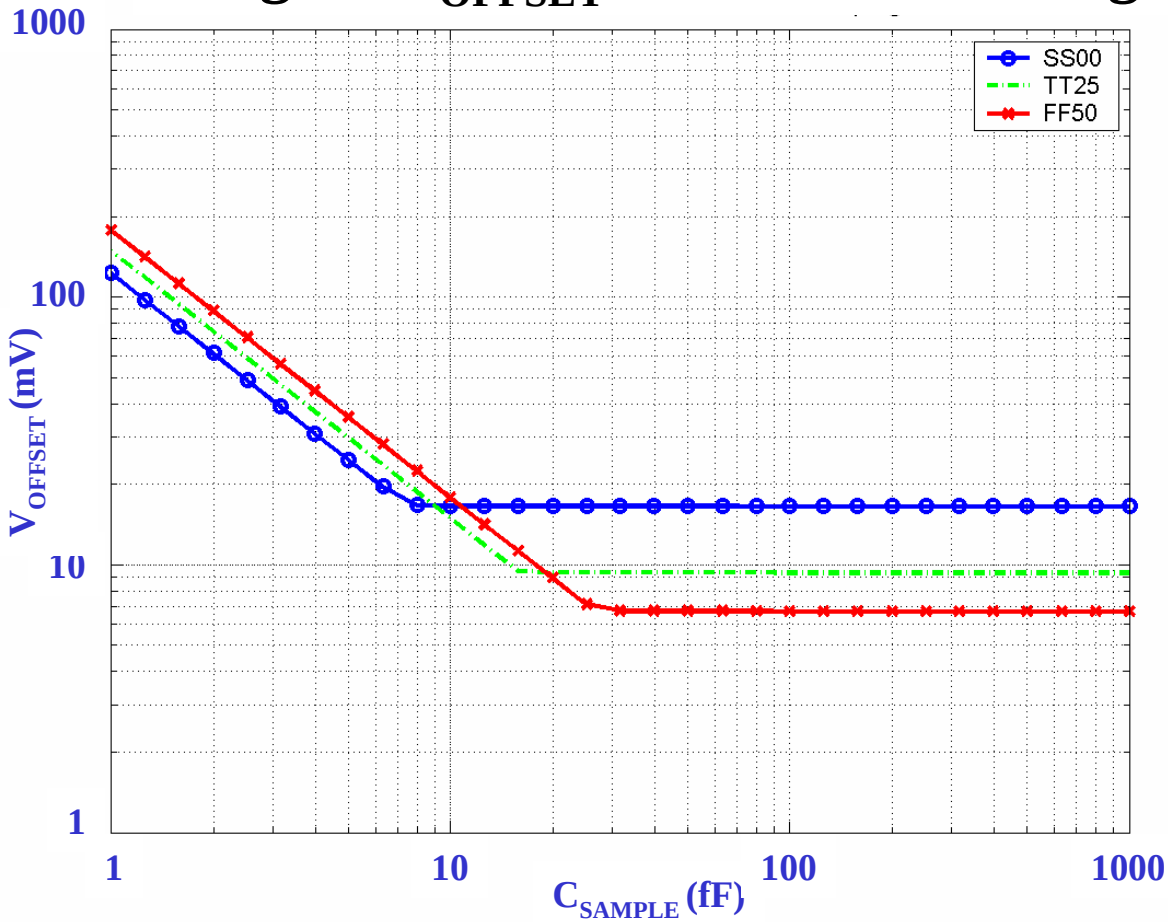
Desirable Functionality:

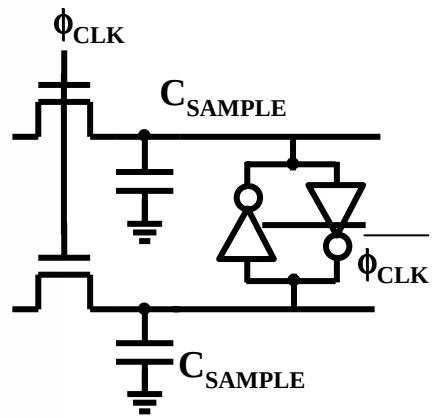
- Minimum Gain = 1,000
- Partition Gain/Stages for Minimum Current Consumption
- Capacitive Coupling Between Stages (Null DC Offset)
- Switch Bias On/Off within T_{WINDOW}
- Fast Overload Recovery (Track Full-Scale 1GHz Sinusoid)
- Additionally Include Filtering for Frequencies < 100MHz, > 1GHz
- Last Stage Drives Sampling Switch Load (could be ~100's fF)



RX: A/D Comparator requirement

1-Sigma V_{OFFSET} for Fixed Tracking BW=1GHz





V_{OFFSET} ~ 20mV (w/ No Explicit Cancellation) for C_{SAMPLE} > 10fF

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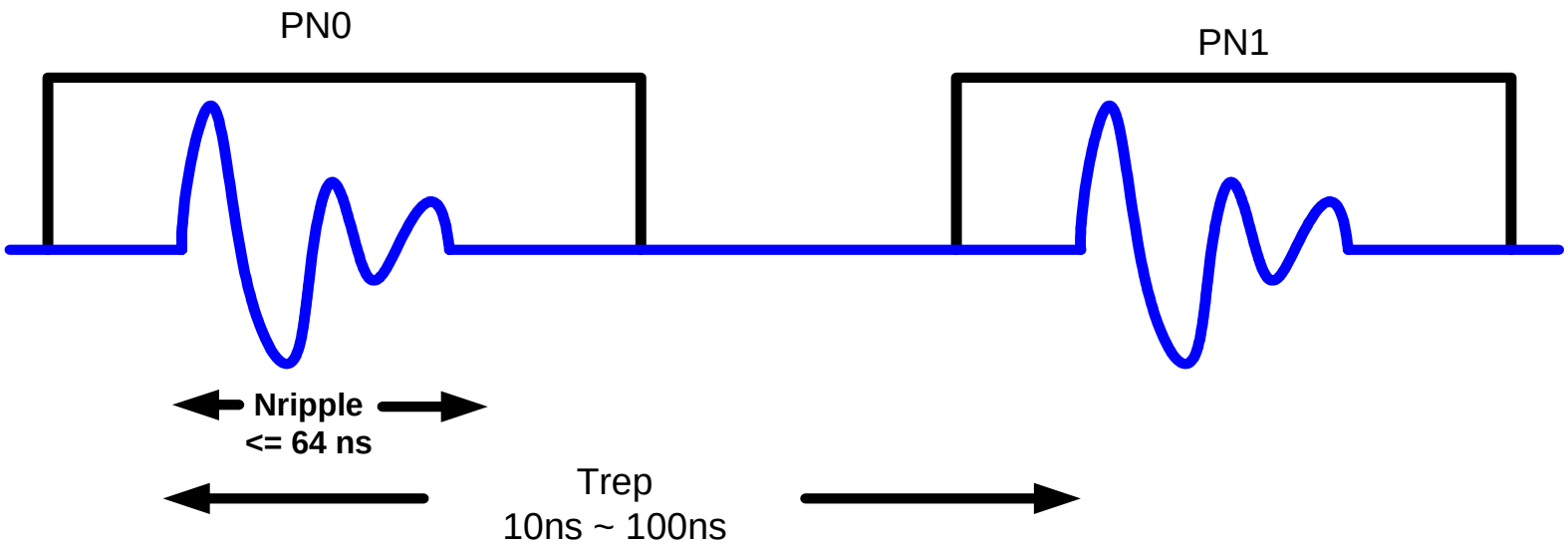
Overview of UWB baseband

Specs for Baseband



- Pulse Repetition Rate: 1MHz to 100 MHz
- Maximum receivable Pulse ripple length ($N_{ripple}=N_{pulse}+N_{spread}$): < 64ns (128 samples)
- Sampling rate: 2 GHz
- PN spread ranges from 1 to 1024 chips

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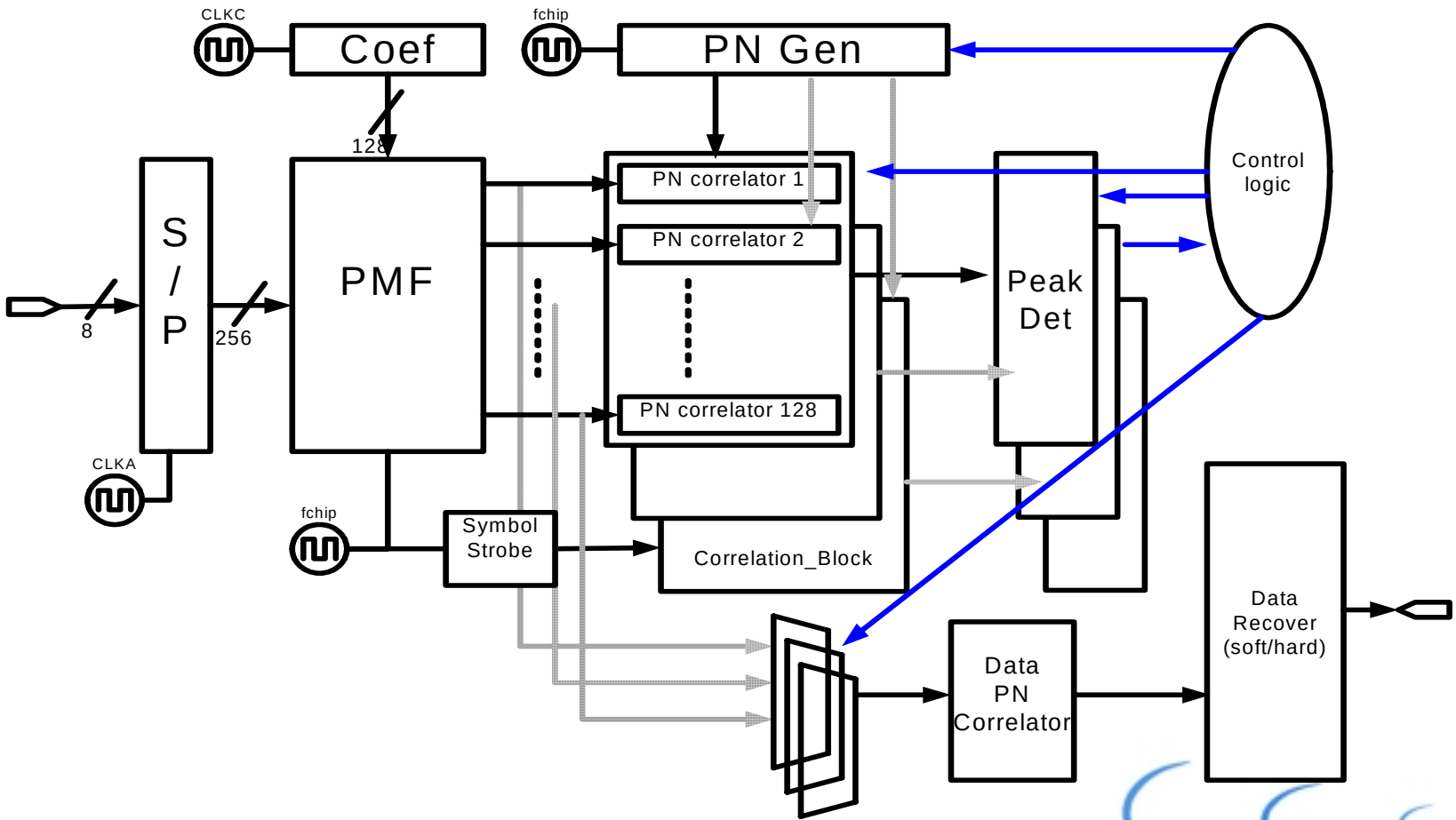
Baseband Overview



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Operation Modes

- ***Acquistion mode:***

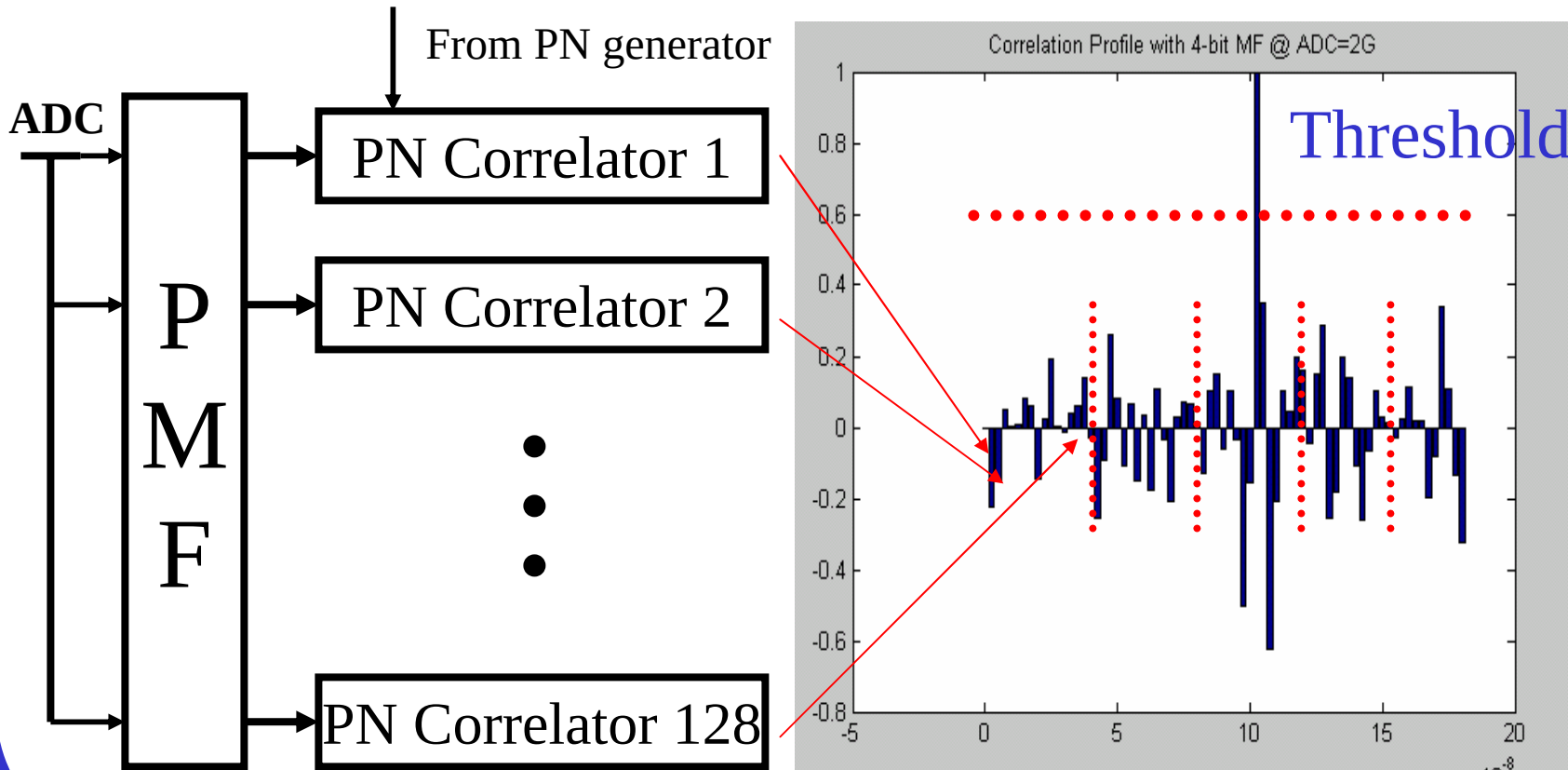
  Receiver tries to lock the signal with a certain PN phase. The implementation uses a mixed mode of parallel and serial search, depends on the tradeoffs between hardware and acquisition time.

- ***Tracking mode:***

  Track the sampling time error caused by the changing channel, sampling clock offset between transmitter and receiver. If the signal is moving toward the boundary of sampling window, it will feedback a control signal to front end to shift the sampling window. And we take the maximum signal to do data recovery.

Acquisition mode

- Searching for the peak at the ouput of correlators



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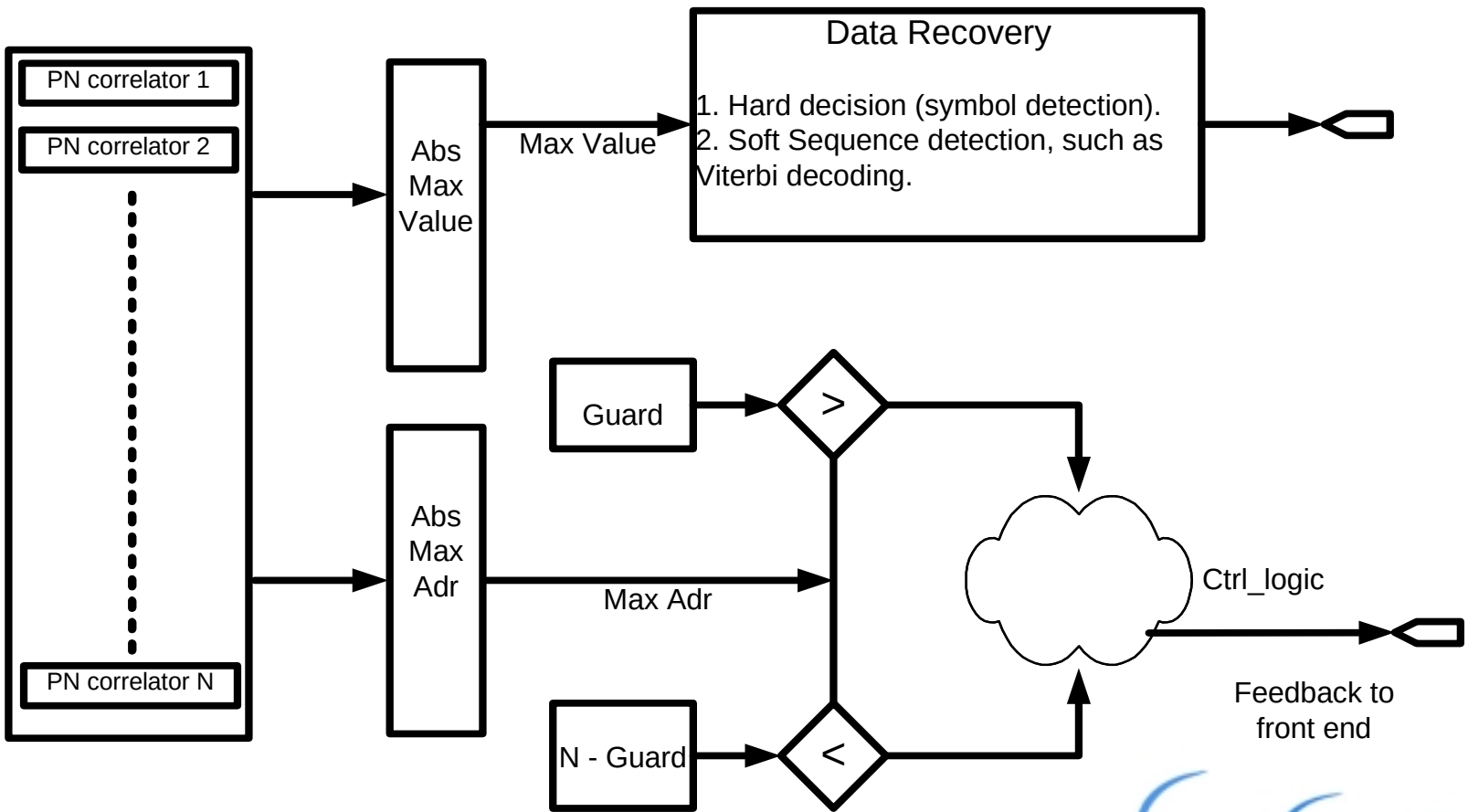
Tracking mode



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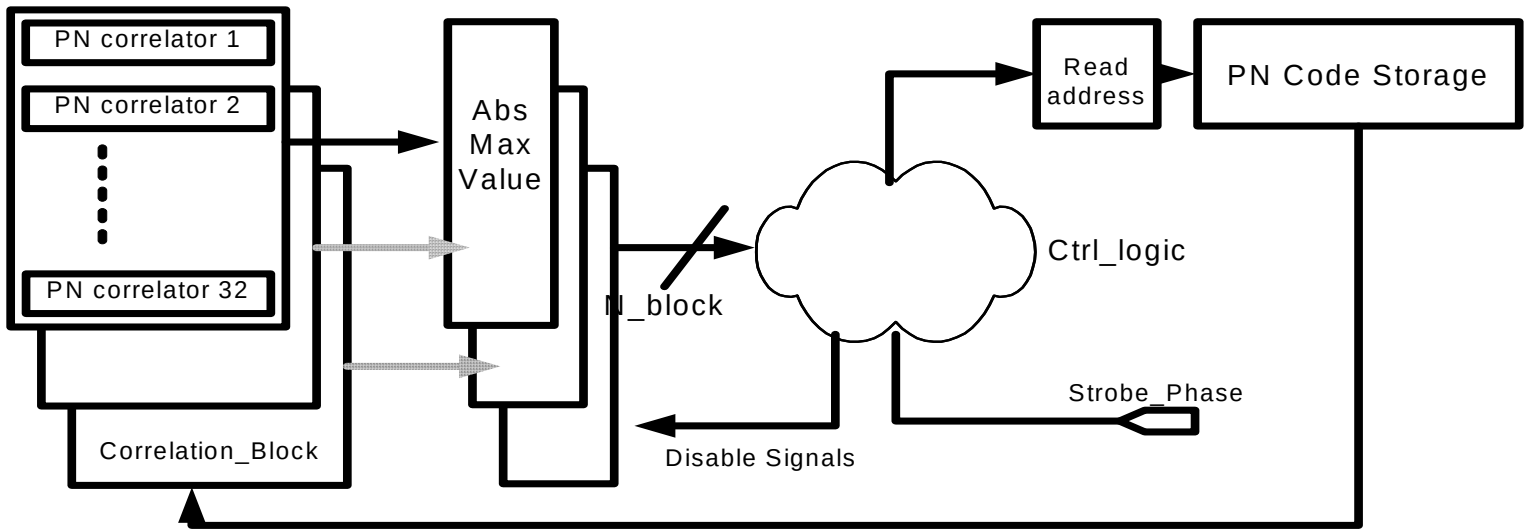
Control logic



- A read clock to fetch the PN phase and a programmable PN length is needed.
- Strobe_phase signal is used to define the symbol boundary after entering tracking mode.
- A enable/disable control bus is needed for gated clock in PN correlators for power saving purpose.

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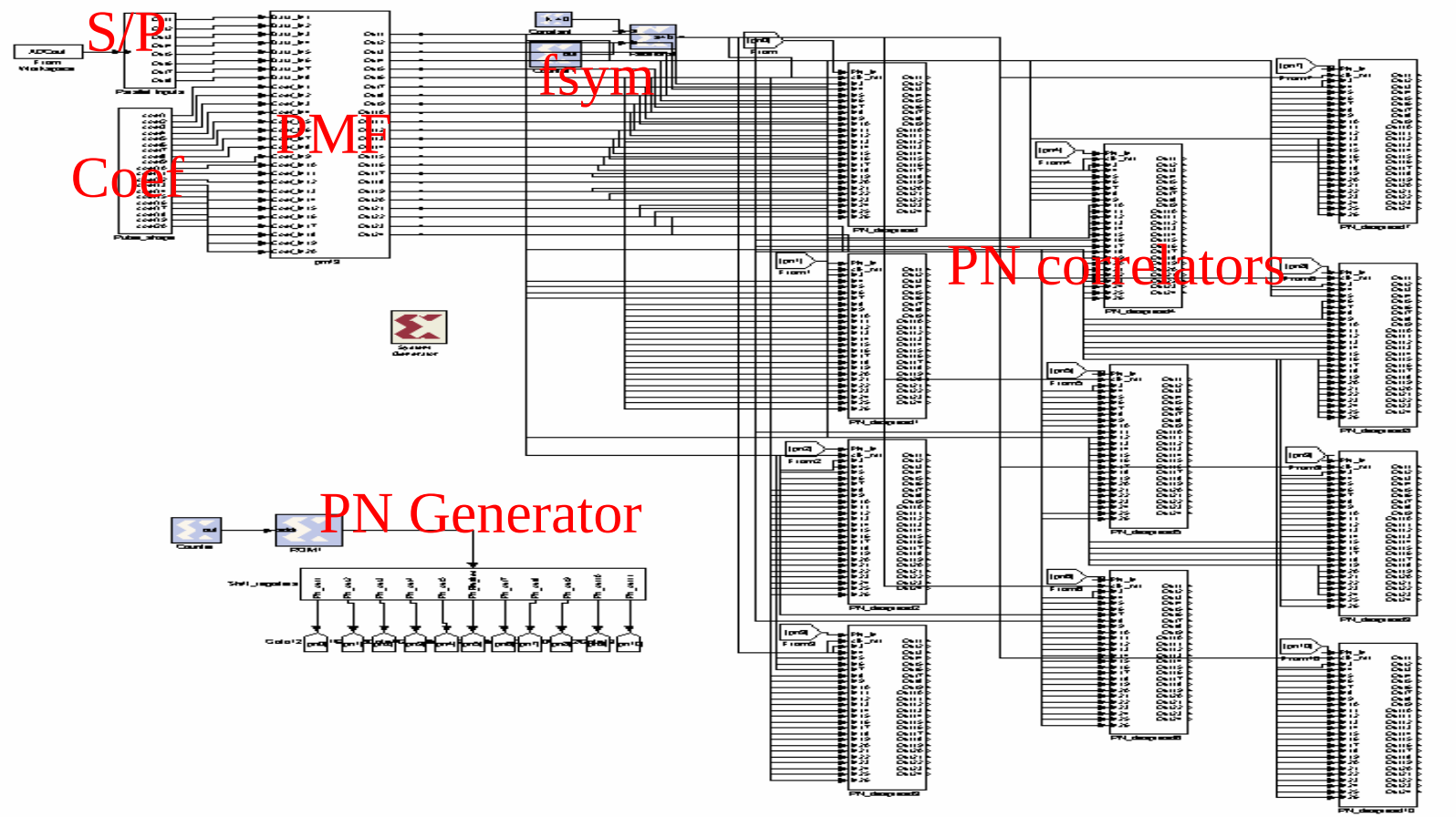
Simulink Implementation



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ASIC Design Decisions

Processing Gain

• For an Input Eb/No = -11dB 1024 chips is more than enough.
(1) Acquisition mode, ~400 chips is enough for suppressing the acquisition error below 1e-3.

Chips	Prob. of Miss lock	Prob. of False alarm	EbNo @ output
300	0.0037	0.0041	14.4245 dB
400	0.86e-3	1.3e-3	15.6643 dB

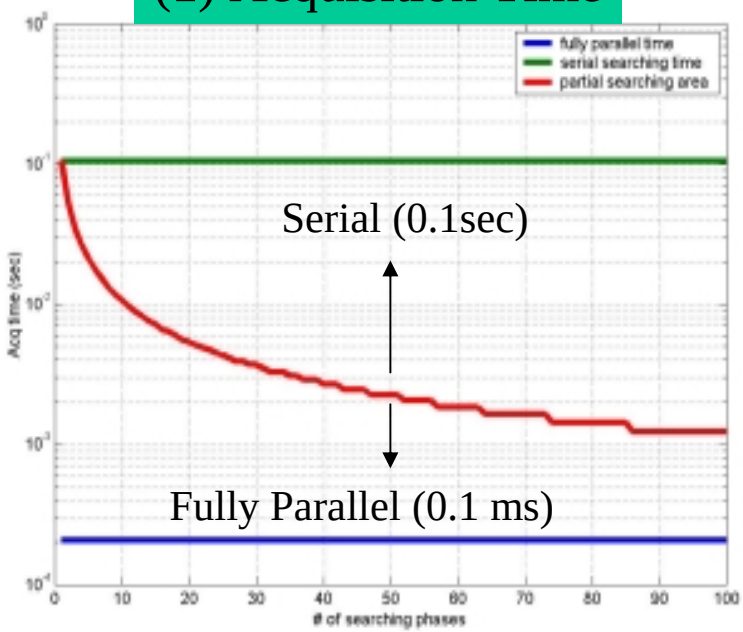
(2) Data recovery mode, ~100 chips could achieve an uncoded bit error rate of 1e-3.

Chips	10	100	200
BER	0.1663	1.1e-3	2e-5

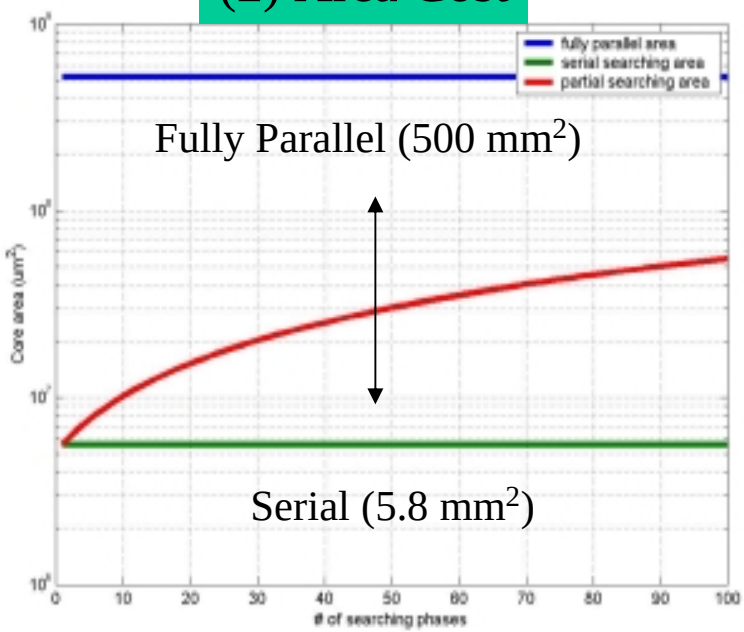
Parallel vs. Serial Acquisition

•Assume the worst case using 1024 PN chips, while pulse rate is equal to 100 ns. We need to choose somewhere in between.

(1) Acquisition Time



(2) Area Cost



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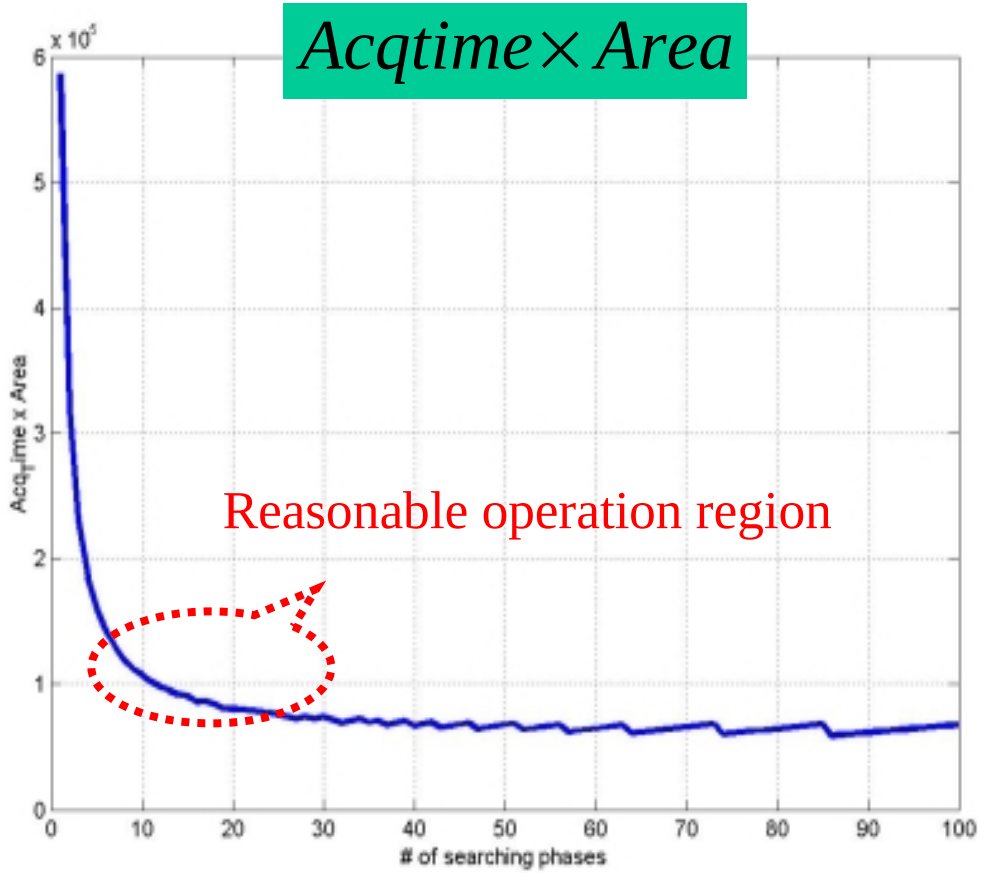
Partial Acquistion

•Once number of parallel search phases are above 10, product of area cost and acquisitior time begins to saturate. Not beneficial to increase more search phases.

• No. of searching phases is chosen to be 11 in the design.



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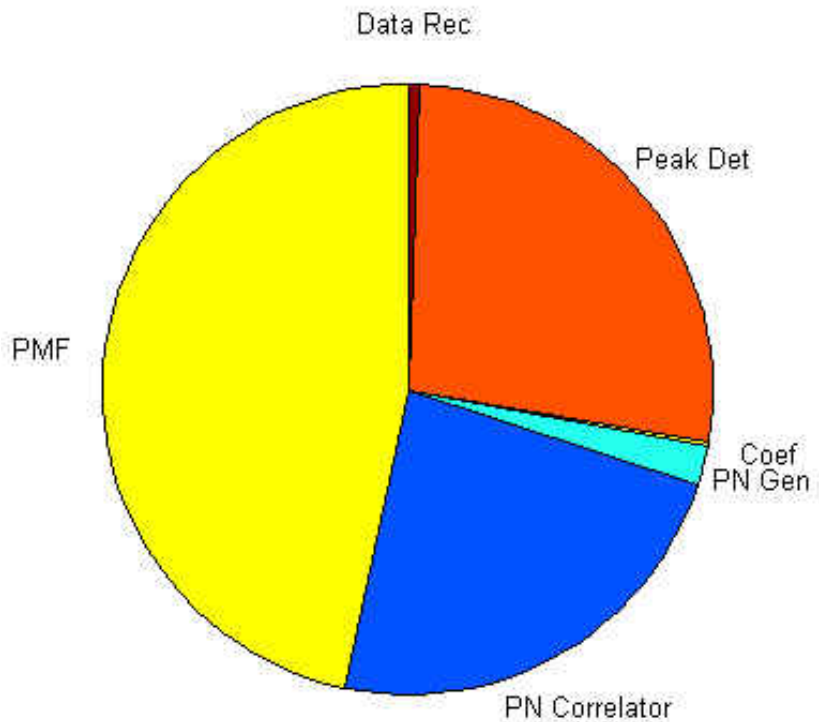
Area and power estimation

Block	Area (mm^2)	Power (Acq)	Power(Track)
Pulse Matched Filter (256 inputs, 128 outputs)	4.95	N/A	N/A
PN Generator (max 1024 chips)	.23	N/A	1.14 mW
Peak detector Block (128 inputs)	2.88	N/A	N/A
Data Recovery (Track 3 samples)	.069	0	54.7 uW
Control Logic (state flow)	<.001	N/A	N/A
PN correlators (contain 128 correlators)	2.47	N/A	0
Total	**10.6**		

Area Distribution on Chip

- The biggest single block is PMF(Pulse Matched Filter), which is implemented in Carry-save adders.
- PN correlators and Peak detectors are proportional to the number of searching phases. The optimal point makes this area comparable to PMF.



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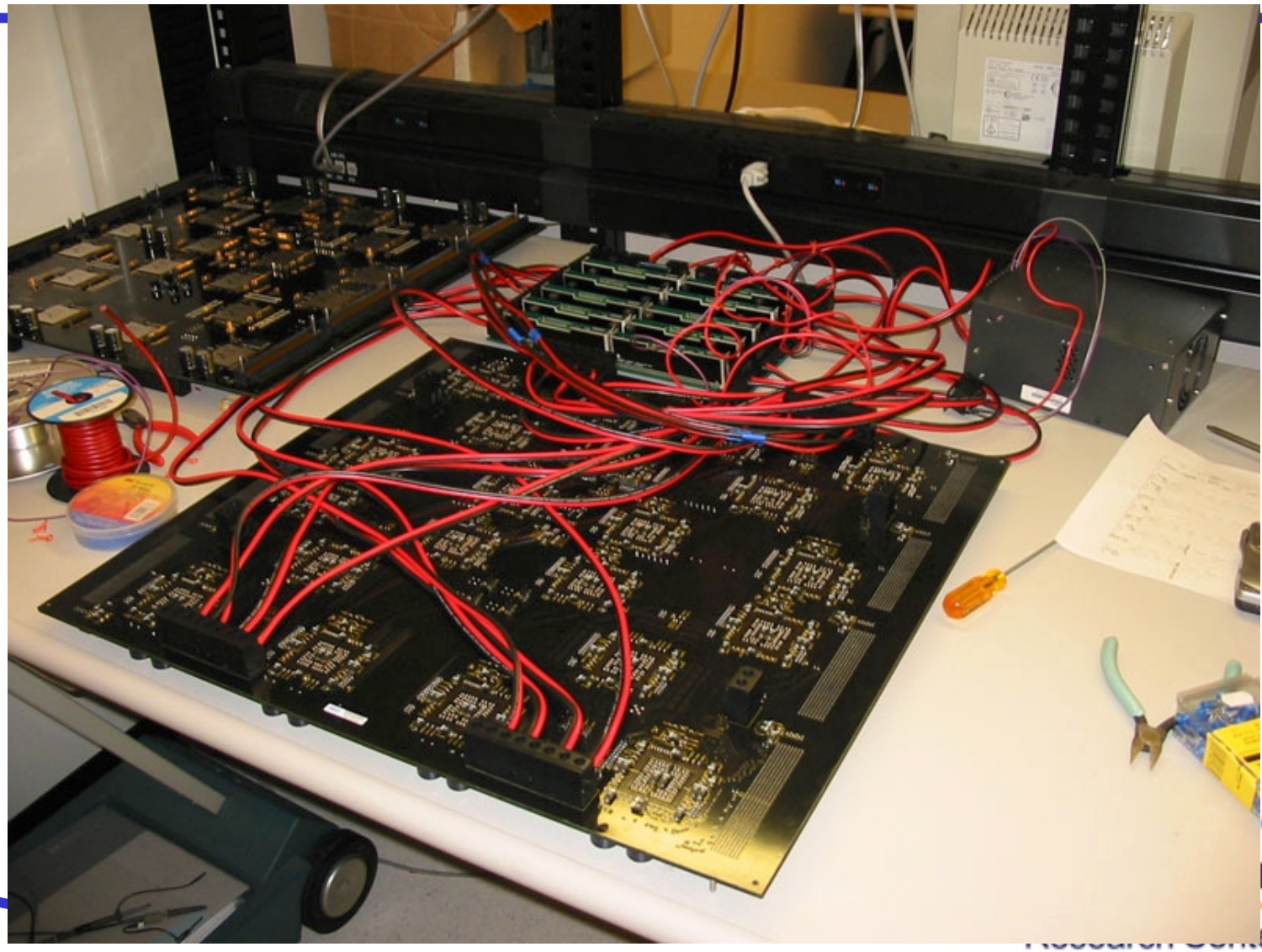
BEE FPGA Array

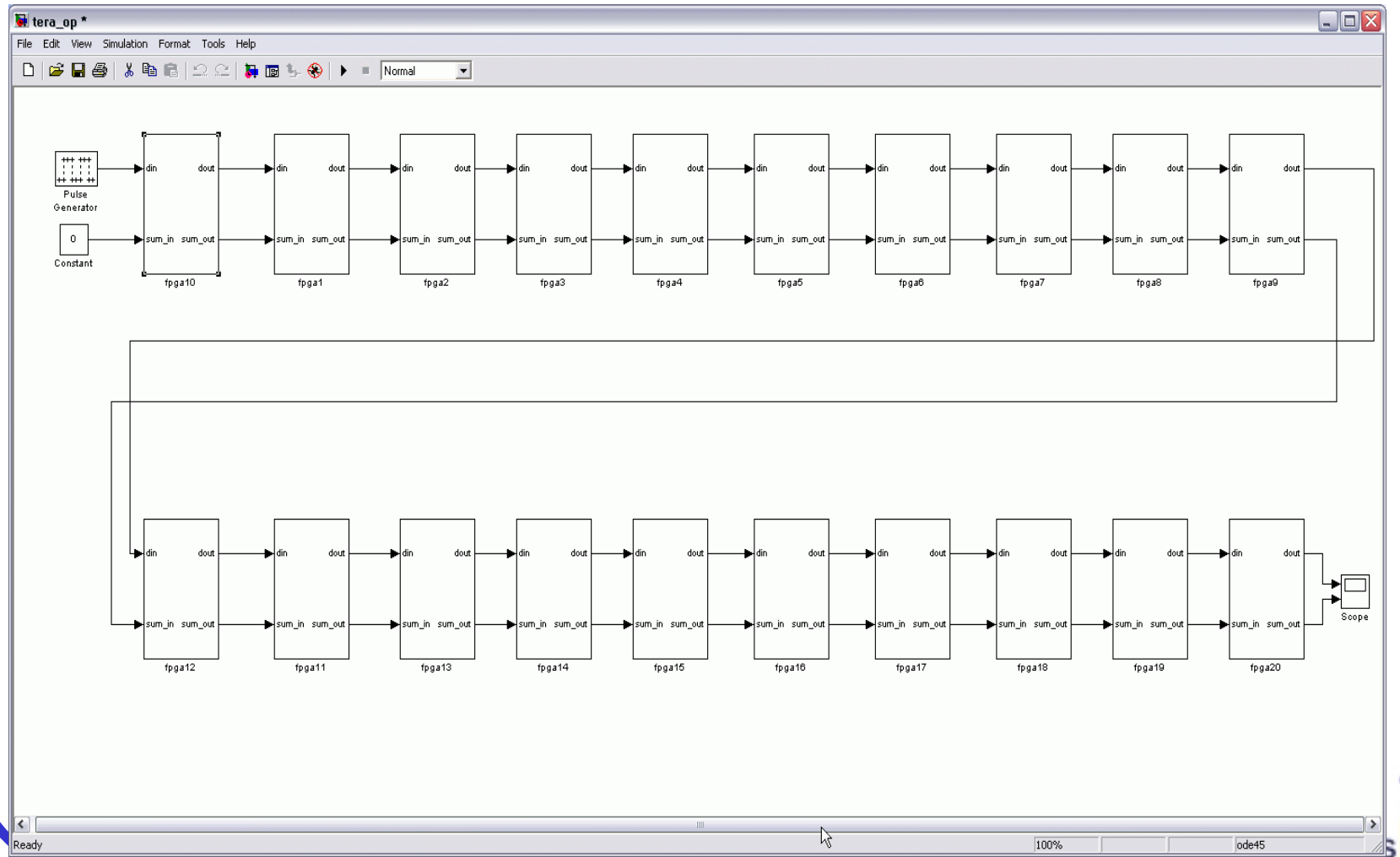
What's BEE?

- A real time hardware emulator built from ***20*** high-density Field Programmable Gate Arrays (FPGAs).
- Emulation capacity of ***10 Million*** ASIC gate-equivalents per module, corresponding to ***600 Billion*** operations (16-bit adds) per second.
- Realistic emulation speed ***10 – 100 MHz***
- ***2400*** external I/O for add-ons, like radios.
- Automated design flow from Simulink to FPGA emulation, integrated with the Chip-in-a-Day ASIC design flow.

Power Board PCB connected to BPU



Simulink - 5120 tap FIR design



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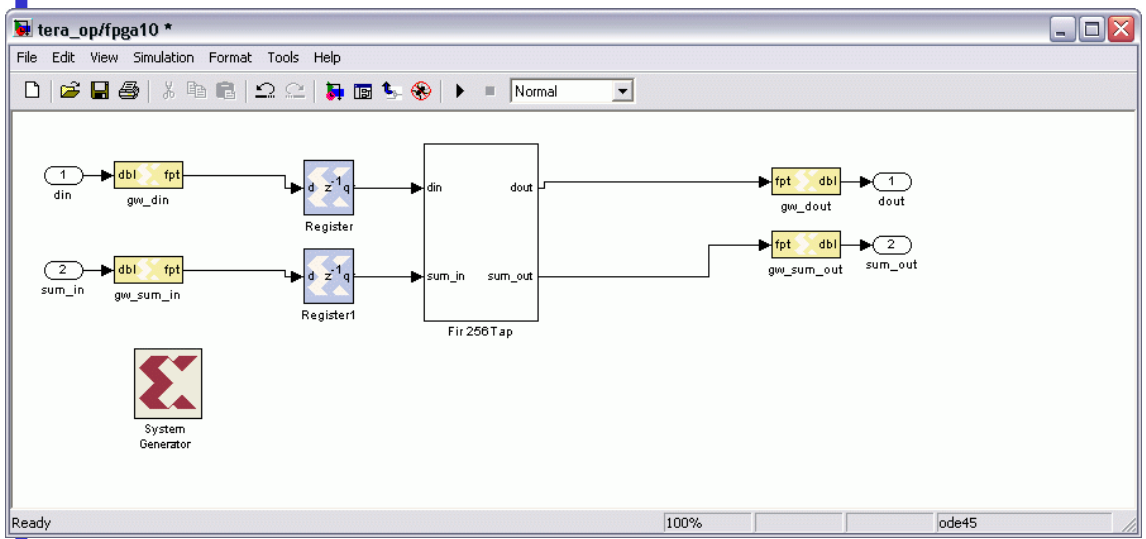
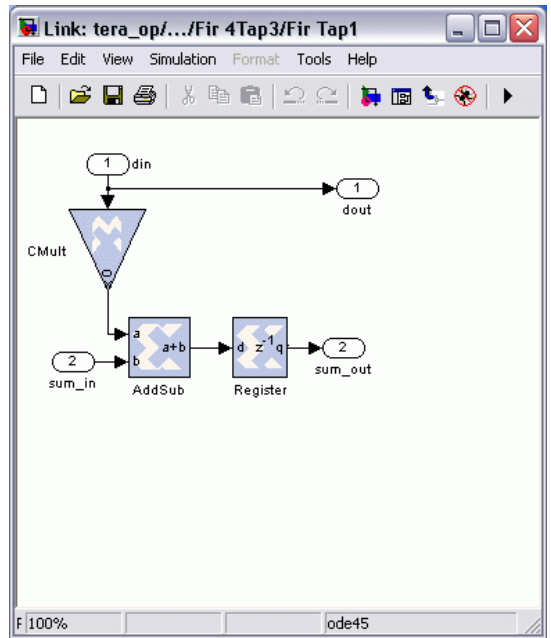
5120 Tap FIR filer design (cont.)





80 MHz sample rate

.8 Teraops/sec

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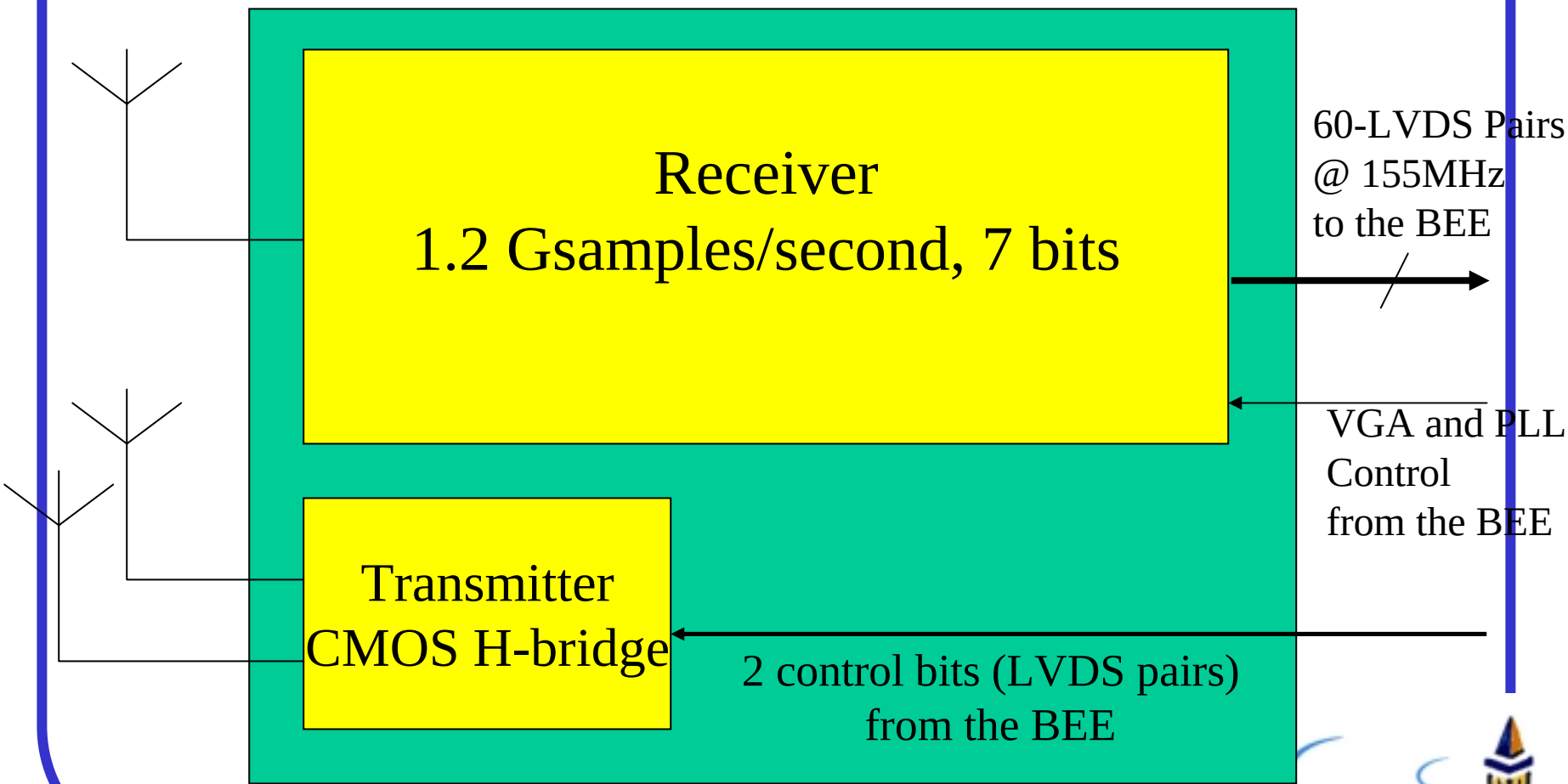
UWB Transceiver Frontend



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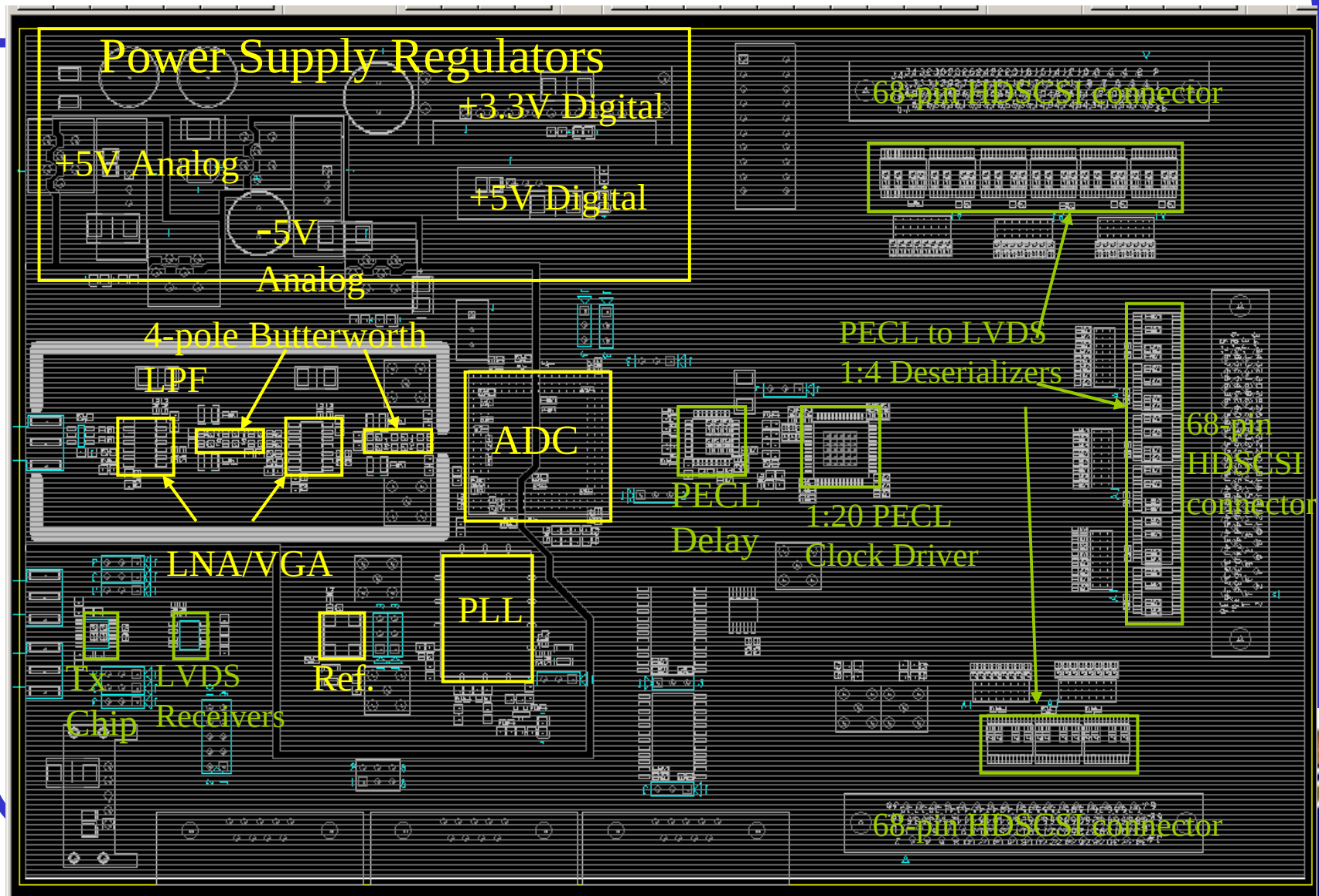
UWB Transceiver board



Status Summary

- First pass system design completed with full simulations
- Analog circuit design approximately 50% completed
- Digital baseband design completed, backend design beginning
- BEE FPGA fabricated and fully functional
- BEE UWB frontend designed