MURI Review Agenda (Afternoon)

1:15 PM: Circuit Design
   Panel: Bob Brodersen, Won Namgoong, Mike Chen, Ian O’Donnell, Stanley Wang
   Topics: UWB Low Noise Amplifier Design in CMOS, low Power Integrated UWB Transceivers, CMOS Implementation Design for UWB Acquisition, Tracking and Detection

2:30 PM: Break

2:40 PM: Future Goals
   Topics: Fundamental Limits on Transient Radiation, UWB Arrays for Direction of Arrival Estimation, Control the UWB Waveform, Multipath-Embracing UWB Time Transfer and Location Techniques, Refined modeling(characterization) of the UWB channel, UWB Performance and CMOS Impairments, Complete Asset Tracking System
   Panel: The UWB MURI Team

3:30 PM: Comments and questions from attendees

4:00 PM: Evaluators' Meeting

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Challenges in Digital UWB Receivers

- High-speed, high dynamic range ADC.
  - Parallel ADC required.
- Wideband LNA.
• ADC sees the full bandwidth of the input signal.
  – Sample/hold circuitry becomes difficult to design.
  – Sensitive to sampling jitter.
• Large dynamic range required in the presence of narrowband interferers.
Frequency Channelized ADC

- ADC input bandwidth reduced.
  - Sample/hold circuitry relaxed.
  - More robust to sampling jitter.
- Reduced dynamic range requirement.
- Sampling jitter and mixer phase noise present.

Jongrit Lerdworatawee, Ali Medi, Won Namgoong
No Narrowband Interferer
Short-Range Ultra-Wideband Systems

Narrowband Interferer Present

[Graph showing the effect of sampling jitter on SNR for different bit resolutions (4-bit and 12-bit).]

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Jongrit Lerdworatawee, Ali Medi, Won Namgoong
Implementation of Channelized Receiver

- A 2-channel LNA/mixer in 0.25um CMOS is currently in fabrication.
- A multi-output frequency synthesizer has been designed.
Research on UWB LNA

1. Understand tradeoffs between LNA gain and NF for wideband signals.
   – Redefine noise figure.
   – Generalize noise analysis of 2-port network.
   – Develop a systematic design methodology for wideband LNA.

2. LNA implementation.
Noise Figure

- Formal definition introduced by Friis (1940s).
  - $\text{NF} = (\text{input SNR})/(\text{output SNR})$.
  - Measures degradation in the SNR as signal passes through the receiving system.

- SNR defined at an infinitesimal frequency band.
  - How do you measure SNR when noise is colored?
Meaningful NF Metric

• Goal of a receiving system in a digital receiver is to condition the received analog signal for digitization.
  – Achieve highest performance after decoding in digital domain.
• SNR should measure performance after the digital decoding process.
  – Metric for a single block, not the entire system.
• Define SNR as the MFB.
  – Achievable performance after digital decoding.
  – NF measures the degree of degradation in the achievable receiver performance.
Effective Noise Figure

- Effective NF obtained by defining the SNR as the MFB.
- The effective NF becomes:

\[ F_{\text{eff}} = \frac{1}{\int \left( \frac{|P(f)|^2}{P_T} \right) \frac{1}{F_s(f)} df} \]

- Analogous to:

- Effective resistance of parallel resistors is dominated by the smaller resistors.
  - Suggests spot NF can be increased in some frequencies for implementation benefits with little loss in performance.
LNA Gain and NF Tradeoff

- Design matching network to optimally trade effective NF with transducer gain.
- Need to analyze noise and gain tradeoff systematically using 2-port network analysis.
  - Problematic in several common CMOS LNA architectures (e.g., inductor degeneration).
• Existing analysis assumes $I_n = I_{nc} + I_{nu}$, $I_{nc} = Y_c \cdot V_n$
  – Incomplete representation.
• Decompose $V_n$: $V_n = V_{nc} + V_{nu}$
  $I_{nc} = Y_c \cdot V_{nc}$; $I_{nu} = Y_u \cdot V_{nu}$
Optimal Matching Network

- At every frequency, optimal gain/NF obtained graphically.
- For wideband matching, solve constrained optimization problem.
  - Minimize effective NF subject to average gain over a frequency band of interest.
  - Assume no structure to solve the lower bound.
- Quantify effectiveness of various matching structures.
- Currently applying these techniques to design LNA for 3-10GHz.
Short-Range Ultra-Wideband Systems

LNA Implementation (in fabrication)

Simulation Results

• Matching Bandwidth: 
  \((S_{11} < -10\text{dB})\) 2.16 – 4.75GHz

• Overall Gain: 15.5 – 12.9 dB

• Noise Figure: 4.5 – 4.4 dB

• IIP3: 6.1 dBm

• Power Supply: 2 Volts

• Power Dissipation: 40 mW

• Technology: TSMC 0.25\(\mu\)m

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Jongrit Lerdworatawee, Ali Medi, Won Namgoong
Implementation Research Projects

- Real-time UWB prototyping infrastructure (Bob)
  - Implementation of BEE FPGA array
  - First pass at UWB front-end
- Implementation of Ultra Low Power - Ultra Wide Band (ULP-UWB) CMOS transceiver
  - System design and simulation on BEE
  - Flexible architecture
    - Variable data rates
    - Programmable codes
  - Analog
    - 2 Gbit/sec A/D
    - Antenna/CMOS LNA
  - Fully parallel digital baseband chip design (Mike)
Short-Range Ultra-Wideband Systems

Implementation strategies (baseband)

Simulink/Stateflow
Description

ASIC Implementation
“Chip in a day”

BEE
FPGA Array

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Bob Brodersen
• Computation rate – 600 Billion ops/sec
• 1600 I/O connections
• Board-level Main Clock Rate: 160MHz+
• On Board connection speed:
  – FPGA to FPGA: 100MHz
  – XBAR to XBAR: 70MHz

• Board Dimension: 53 X 58 cm
• Layout Area: 427 sq. in.
• No. of Layers: 26
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BEE in Chassis with I/O

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Bob Brodersen
16dB-26dB
Gain Control Range

The output lines of the deserializers operate at **155MHz**.

DATA_READY bit from ADC is used to clock deserializers at **622MHz**.

Note: The programmable delay is needed to properly position the clock relative to the data transitions, so that no setup or hold time violations will occur at the input registers of the deserializers.
Short-Range Ultra-Wideband Systems

Transceiver PCB

Power Supply Regulators

+5V Analog  -5V Analog

+5V Digital

ADC

4-pole Butterworth

LNA/VGA

PLL

Delays

1:20 PEC

Clock Driver

PECL to LVDS Deserializers

68-pin HDSCSI connector

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Bob Brodersen
Prototyping Hardware Status

- BEE operational and in use for verification of digital baseband circuitry
- First pass of UWB transceiver completed and second version in design
  - Increasing bandwidth to 1 GHz (2.4 Gbit/sec A/D conversion)
  - Using fiber links between BEE and analog transceiver
    - Electrical isolation
    - Higher digital bandwidth (20 Gbits/sec)
Chip implementation

• Digital design verified in BEE
• Analog design completed and beginning layout

Remaining talks on this activity:
  – Ian: Chip architecture and critical design issues
  – Stanley: LNA and pulser
  – Mike: Digital baseband design
UWB Integrated Transceiver Project

Targeting Sensor Network Application

Specifications:
• 100kbps over 10m with $10^{-3}$ BER
• 1mW total (TX+RX) power consumption
• 0-1GHz bandwidth

First All-CMOS Integrated UWB Transceiver
Aggressive Low-Power Design
“Mostly-Digital” approach, simplify analog front-end
Provide Flexible Platform for Further Research

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Ian O’Donnell, Bob Brodersen
Parallel Sampling of a Window of Time

\[ T_{SAMPLE} \]
\[ T_{WINDOW} \]
\[ T_{PULSE\_REP} \]

\[ T_{SYMBOL} \]
Short-Range Ultra-Wideband Systems

UWB Transceiver Architecture

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Short-Range Ultra-Wideband Systems

Performance: Throughput/Power

Published Results:
- CMOS UWB Potentially 10x Better
- Throughput/Power (kbps/mW) vs. Pulse Rep Rate (Hz)
  - 100 kbps/mW
  - 10 kbps/mW
  - 1 kbps/mW

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Quantify Effects of Hardware Impairments:

- Analog to Digital Conversion Bitwidth
- Matched Filter and post-Correlation sizes
- Timing Requirements:
  - Precision (Matching between TX and RX)
  - Accuracy (Jitter)
A/D Sampling Bitwidth

1-bit A/D Is Adequate

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Matched Filter Tap Bitwidth

5-bit Coefficients Are Adequate
Oscillator Accuracy (Matching)

For:
- Drift < 100ps Over Symbol

Crystal is Required

- 10 PPM
- 1000 PPM
- 0.1%
- 10% Precision Component
- Crystal
- TCXO

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Oscillator Precision (Jitter)

For:
RMS Jitter < 25ps Over Symbol

Crystal is Good

-90 dBC/Hz @ 0.1% of \( f_c \)

-120 dBC/Hz @ 0.1% of \( f_c \)

Ring Oscillators

LC Oscillators

Crystal Oscillators

Phase Noise (dBC/Hz at 0.1% of \( f_c \))

1.6 MHz

10^4 10^5 10^6 10^7 10^8 10^9 10^10

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Short-Range Ultra-Wideband Systems

UWB CMOS Transceiver Status

Status:
System Design Complete
Analog Circuit Design Complete
Digital Design Complete and in Verification Stage

To Do:
Analog Layout
Merge Analog/Digital into Single Die
Top-level testing

Tape-out in next couple months.

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Ian O'Donnell, Bob Brodersen
Introduction

• Pulse generator and low-noise amplifier are circuits interfacing with antennas
• Basic properties of UWB antennas have to be known
Short-Range Ultra-Wideband Systems

Small Loop Antenna Example

- For indoor wireless applications, antennas have to be small
- Small antennas have simple equivalent circuits
- Curve-fitting the input impedance
  - Only ONE RESISTOR
- Use the terminal voltages to help design the driver/LNA

E-Field

Small Loop Antenna

Vin

Rrad

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USC UltRa Lab
UMass Antenna Lab
Stanley Wang, Bob Brodersen
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UWB Pulse Generation

- Large Current Radiator (LCR) as the TX antenna
- Low-pass filter for pulse-shaping & FCC radiation mask

- H-bridge pulser to drive inductive load
- Flexible driving force by parallel structure

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H-bridge Operations (Transmit ‘0’)

- EP0 & EN0 turned on
- Current flows from Vdd to Gnd thru LCR
- Fast-rising voltage at LCR terminals generates a positive Gaussian pulse

- EN0 off and EP0 on
- Current flows back to Vdd
- Fast-falling voltage at LCR terminals generates a negative Gaussian pulse
Low-Power Pulse Generator Design

- Intervals of doublets affects the width of the frequency lobes, but total power radiated keeps the same.
- The smaller the interval, the smaller the power consumption and higher the efficiency.

Stanley Wang, Bob Brodersen
Short-Range Ultra-Wideband Systems

UWB Receiver Front-end

- Waveform of the source imitates the radiated E-field
- Source impedance equal to antenna input impedance
- LNA $\rightarrow$ Matching Network

$\text{Loop Antenna}$

$\text{Matching Network/Filter}$

$I(t) = a \cdot E(t)$

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• **Specifications**
  – Fully-differential for on-chip interference immunity
  – Voltage Gain > 15dB
  – 3dB BW : 0.1~1GHz
  – NF < 6dB
  – Linearity : doesn’t matter
  – Constant group delay
  – Input impedance : 50ohm
  – **Goal : Minimize power consumption (< 1mW)**
• **Low input impedance sets the power consumption**
• **What LNA topology should be used?**
Short-Range Ultra-Wideband Systems

Existing Wideband LNA

R-terminated

\[ \text{Rin} = \text{RT} \]

Shunt-Feedback

\[ \text{Rin} = \frac{Rf}{1 + \text{gmRL}} \]

Common-Gate

\[ \text{Rin} = \frac{1}{\text{gm}} \]

- Resistive-terminated LNA has very bad NF
- Shunt-FB and CG LNA’s need \( \text{gm} = 40\text{mA/V} \) which makes sub-mW power consumption unfeasible
Current-Reuse Technique

Shunt-Feedback

- PMOS are added in as amplifying devices
- No extra DC current
- $G_m = g_{mn} + g_{mp}$
- $R_{in}$ is halved
- Voltage gain is doubled
- NF decreased by 3dB
- BW decreased but OK
- $R_{in} = 1/(g_{mn} + g_{mp})$
- $R_{in,\text{diff}} = 2/(g_{mn} + g_{mp})$
- Still burn > 1mW

Common-Gate

- $R_{in} = 1/(g_{mn} + g_{mp})$
- $R_{in,\text{diff}} = 2/(g_{mn} + g_{mp})$

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FB/CG Hybrid LNA

- $M_{p1}/M_{n1}/R_{f1}$ act as FB Amp to $V_{in+}$ and CG Amp to $V_{in-}$
- $M_{p2}/M_{n2}/R_{f2}$ act as FB Amp to $V_{in-}$ and CG Amp to $V_{in+}$
- $R_{in} = 1/ [2*(g_{mn}+g_{mp})]$ 
  For $R_{in} = 50\text{ohm}$,
  $g_{mn} = g_{mp} = 5\text{mA/V}$
  $\rightarrow$ 8 times smaller than $40\text{mA/V}$ in CG or Shunt-FB amplifier!
  $\rightarrow$ sub-mW LNA feasible
- $A_v = 2*(g_{mn}+g_{mp})*R_f$

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• Back-gate Cross-coupling enhances Gm by 10%

• Power = 0.61mW

• All the specs are met

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- ST Microelectronics 0.13um CMOS triple-well process
- Layout area: 59um x 45um
- Common-centroid layout for good transistor matching
- Dummy for good resistor matching
- Capacitors not shown
Short-Range Ultra-Wideband Systems

Why Dedicated ASIC for UWB?

Here we are!

General Purpose DSP

Dedicated

MOPS/mW

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Mike Chen, Bob Brodesen
What does Baseband do?

- **Fuctionality:**
  acquisition; ML detection; early/late tracking

- **Target:**
  sufficient flexibility & low power!

- **Pulse Repetition (Clocking) Rate:**
  30 MHz to 1 MHz

- **Maximum Raking Length**
  \(T_{\text{rake}} = T_{\text{pulse}} + T_{\text{spread}}\): < 64ns (128 samples)

- **Additional Processing Gain**
  0 to 30 dB
Flexible Low Power Architecture

- Fully parallel matched filter (FIR), and PN correlator structures
  → High area and power efficiency without time multiplexing
- Ability to turn down the unused transistors for 10x power saving in tracking mode
- Programmable matched filter response and PN codes
- Duty-cycled and continuous operation modes
Parallel v.s. Serial Searching Scheme

- Assume 1024 PN chips, 10 MHz pulse rate.

1. Acquisition Time
   - Serial: 0.4 sec
   - Fully Parallel: 0.4 ms

2. Area Cost
   - Fully Parallel: 500 mm²
   - Serial: 5.8 mm²

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Short-Range Ultra-Wideband Systems

Design Methodology

- Develop algorithm in Matlab/Simulink, BEE and ASIC implementations start from Simulink netlist.
- Datapath is synthesized and explored in Module Compiler.
- Control logic is designed in StateFlow, and later translated by SF2VHD.
- Massive parallel and structured processing elements requires 31 meters of wires!
  → Hierarchical front end and physical design.
Design Flow

Develop Algorithm  Front End Design  Verification  Backend Physical Design

Matlab Test Vector

Algorithmic: Simulink Schematic

XSG

BEE

Module Compiler

Gate VHDL

State Flow SF2VHDL

Top-level VHDL

Behavioral VHDL

Synthesis & Optimization: Design Compiler

Bottom Up/Top Down hierarchies

Gate VHDL

Gate Verilog

Modelsim

Gate Verilog

End of FE

End of FE

FP & Place: First Encounter

Hierarchy Placement

Power Strap Cmd

Route: Nanoroute

DEF

Final Verilog

SPF/SDF/set_load

EPIC Verify

ST A Path Mill

Func, Power -> Nanosim

GDS

VCD

VCD

CDL netlist

CDL for ST lib.

GDS

Filter Spice

Design Spice

CDL for ST lib.

Calibre DRC/ Antenna Rule

Calibre LVS

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Graphic View of Flow

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**UWB Baseband Chip Status**

**Process:** 0.13um (ST Microelectronics)

**Size:** 3.6mm x 3.3mm

**Standard Cells:** 530,000

**MOPS/mW:** 1,483

**Power:**
- **Acquisition** $\Rightarrow$ 12 mW
- **Tracking** $\Rightarrow$ 1.5 mW
  
  @ 1.08 V, 10 MHz clk
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