On-chip Automatic Direct Tuning Circuitry Based on the Synchronous Rectification Scheme for CMOS Gigahertz Band Front-End Filters

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ABSTRACT

A new automatic tuning circuit based on synchronous rectification scheme is proposed and functions in the idle periods between the burst-mode transmissions. The proposed CMOS tuning circuit can be fully integrated with the front-end filter. Simulation results employing 0.5μm CMOS technology have verified that the center frequency is automatically tuned to 1.25GHz with 10% process variation presence. The deviation is 15MHz, representing to only 1.2% error.

1. INTRODUCTION

The increasing command for wireless communication necessitates low lost, high integration level, and high performance solutions to be implemented in radio frequency (RF) front-end systems. While GaAs and BiCMOS technologies are employed to achieve higher operating frequencies and low noise performance, considerable research has been conducted in developing CMOS monolithic RF systems as it would allow integration of other digital signal processing circuits, leading to a single-chip solution. In telecommunication applications, gigahertz band CMOS front-end filters with high quality factors (Q) have been proposed in the literature [1][2][3][4], but practical automatic tuning systems have not yet been exploited. Automatic tuning remains a challenging research area.

The performance of fully integrated analog filters usually deviates from the filter design specification due to fact that exact value components are not obtainable to guarantee the characteristics of the filters typically used in narrow band applications. In addition, active devices are more sensitive to temperature fluctuation than passive elements, leading to severe performance errors. A solution to this problem is to use an accurate external reference signal (e.g. master clock) to tune the filter. The master-and-slave scheme [5][6][7] is a widely-used tuning circuitry for medium-Q video band active filters. The MASTER is designed to model all the relevant behaviors of the main filter SLAVE. The MASTER, basically the duplication of the SLAVE, can be the voltage-controller oscillator (VCO) or voltage-controlled filter (VCF) [8][9] type of configurations. The MASTER is continually tuned to the desired frequency by using phase-locked loop techniques and the frequency-controlled voltage simultaneously feeds to both MASTER and SLAVE. Q tuning can be achieved in the similar approach [9]. The accuracy of the indirect tuning heavily relies on the matching and tracking between both filters. However, the parasitic effects in the CMOS high-Q gigahertz band filter are very large and can not be matched well. In addition, the cost of the extra tuning circuitry needs to be minimized, such as the silicon area, noise, power dissipation, and interference between the reference signal and the SLAVE filter. Furthermore, the design of the front-end bandpass filters usually employs LC tank and, as we know, monolithic passive inductors consume considerable silicon area. Therefore, another tuning scheme is demanded.

The Q tuning for correcting the temperature fluctuation has been reported in [10] by employing the input bias temperature compensation technique. However, problems with process variation have not been resolved yet.

This work presents an automatic direct center frequency tuning scheme called synchronous rectification for CMOS front-end filters in the gigahertz range operation. This tuning circuitry is simple, low power, small silicon area, and fully-integrated. The same scheme also can be applied to the image-reject filters.

2. TUNING SCHEME AND FILTER

2.1 Synchronous Rectification Tuning Scheme

In most hand-held transceivers, the limited isolation between the transmitter and receiver prevents simultaneous transmission and reception. The transceivers are normally operated in a half duplex mode, with the transmitter and receiver being used alternately. As a result, the receive filters can be tuned while the transmitter is operating. After filters are tuned to the desired frequencies, filters are then switched back to the main receiving paths for normal operation.

The conceptual block diagram for this proposed tuning scheme is shown in Fig. 1. Two clocks are employed in this scheme. First, CK1 is selected as an input signal to the bandpass filter and the corresponding waveform is generated. The peak detector detects the peak amplitude V1, and then SW slowly switches the input to CK2, obtaining another corresponding peak amplitude V2. Therefore, only one of the two clock frequencies CK1 or CK2 is used as an input signal to the bandpass filter by switching SW. CK1 and CK2 are selected symmetrically below and above the desired center frequency. The difference ΔV between V1 and V2 depends on the deviation between the "current" center frequency and desired center frequency. The frequency tuning voltage V_f is computed by feeding both ΔV and SW to the multiplier. A integrator is employed to obtain a

high gain and filters out the high frequency harmonics generated by the multiplier. V_f then varies the DC bias voltage in the varactor of the bandpass filter, leading to the change of the center frequency. Note that a SW delay circuit is intentionally inserted to balance the two signal propagation paths, leading to more accurate multiplication results. The tuning process is repeated until V_f is settled to a stable value, so that the desired center frequency fo=(CK1+CK2)/2. This synchronous rectification tuning scheme allows us to use the correlation between the filter output and SW to form a negative feedback system. In this work, CK1 and CK2 are chosen –12 dB below the peak value of the center frequency amplitude response. Fig. 2 sketches three possible tuning situations and how to use multiplication unit to determine the correct tuning direction for V_f to tune the filter.

2.2 Tuning Circuitry

The selection of the input stimulus is illustrated in Fig. 3. Only one of the two input test signals CK1 or CK2 is selected to pass to the bandpass filter by Ma and Mb. A large voltage swing SW1 with 50% duty cycle is required. While Ma or Mb is ON, it conceptually forms a short circuit, allowing CK1 or CK2 to charge the capacitor Cg. The output test signal is then fed to the input of the bandpass filter.

Fig. 4 illustrates a LC bandpass filter designed for this tuning process. The cascode input stage provides good isolation between input and the following stages, improves stability, and reduces Miller Effect. A monolithic inductor with resistive loss r_p and parasitic capacitance to the substrate C_p is resonant with a poly capacitor C and a voltage-controlled varactor Cvar, generating a second-order bandpass response. Monolithic inductors are well know for requiring a large area and providing a low inductor Q. Therefore, a negative resistance generator formed by M5 to M7 is used to compensate the loss, leading to a high-Q filter. The bias circuit consisting of M3 and M4 provides 50 ohm input impedance to the antenna. Since the center frequency fo is determined by LC, it can be tuned by varying the varactor value Cvar by tuning V_f. In addition, Q can be tuned by varying the negative resistance by tuning V_q. Thus, we emphasize only the frequency tuning in this paper. Vout_BP is the regular output port for the communication channels and its DC bias is set up for proper peak amplitude detection in the tuning process. The bandpass filter has been designed to have a center frequency at 1250Mhz with Q=30, 23.6dB voltage gain, 5.2dB noise figure, -15dBm IIP3, and 23mW power dissipation. A 4.1nH inductor L and a 6pF capacitor C are employed.

The peak detector depicted in Fig.5 consists of a source follower with a charging capacitor C1 and an additional low pass filter formed by R3 and C2, leading to considerable gain attenuation for high frequency signals. The time constant is arranged to filter out CK1 or CK2, but basically maintains SW transitions. M15 provides extra gain with reasonable linearity. Illustrated in Fig. 6 is the SW generation. SW1+ and SW1- are generated to provide proper switching activities to the Fig. 3. The delay elements consist of M37 to M40 with loading capacitors C3 and C4, providing roughly 15ns delay. Voltage swing reduced circuit formed by M41 to M47 provides proper voltage levels around 500mVp_p to drive the multiplier. SW2+ can be generated in the similar fashion by adding another inverter stage before the swing reduced circuit.

A Gilbert cell is used in the multiplication circuitry due to the simple and balanced architecture. Since four-quadrant multiplication is required for the synchronous rectification, differential input signals need to be generated. Here, we use $R_{\_LP}$ and $C_{\_LP}$ to form a lowpass filter, leading to the same DC bias voltage for the gate terminals of M53, M54, M73, and M74. Differential signals can be created due to the common-mode rejection of a differential pair. A source-degeneration resistor R54 helps to increase the input linear range. Switching pairs M59 to M62 are designed to operate as ON or OFF state to provide a maximum gain for this stage. Transistors M71 to M82 are duplicated circuitry from M51 to M62, providing a DC voltage level to the integrator for comparison in Fig. 8.

2.3 Simulation Result

The target central frequency 1250MHz is selected as a test vehicle. Two input testing signals with amplitudes –12dB below the peak amplitude of the central frequency are 1203MHz and 1297MHz and both generate 60mV to the input port of the bandpass filter without causing much distortion. Fig. 9 shows the outputs of the bandpass filter and peak detector. It can be observed that the amplitude difference of two input signals is gradually converged almost zero. The SW signals generated to the selection of the input signals and multiplier is shown in Fig. 10. The inductor is changed from 4.1nH to 3.7nH to simulate 10% process variation and let the tuning process to correct this error. Fig. 11 shows the tuning voltage settles to 1.255V, corresponding to central frequency at 1265MHz; this leads to 1.2% tuning error.

Care should be exercised to ensure balanced timing delays in both signal tuning paths. The precision of the tuning basically relies on the choice of the center frequency, peak detector, the offset voltage of the multiplier, and the open-looped gain of the integrator. Although the bandpass filter functions at gigahertz frequency range, the following voltage buffers and the peak detector have limited frequency responses, leading to peak amplitude detection error. Therefore, higher frequency test signal (CK2) can not be arbitrarily high. Iterative simulations need to be performed to locate the appropriate value. In addition, a simple CMOS peak detector can not detect faithfully the true amplitude of the output voltage from the bandpass filter if the incoming signal or the difference of two signals is small. The offset voltage in the multiplier could cause problems too. Proper transistor sizes and layout techniques are required to minimize this effect.

3. SUMMARY

Scaling down the dimensions of transistors and achieving the maximum integration level by incorporating as many circuits as

possible in a chip are inevitable trends for RF circuit design. Currently, only few components are integrated with other digital circuitry. The proposed tuning scheme can be fully integrated monolithically, eliminating the requirement of post tuning process [4].

Based on the tuning in the idle periods between burst-mode transmissions, a synchronous rectification scheme is proposed to automatically tune the front-end bandpass filter. After the tuning process is finished, the filter is tuned to the desired center frequency and the tuning circuit is decoupled from the filter. Then the normal communication channels are reconnected and the filter starts receiving the incoming RF signals. Since this tuning scheme directly tunes the filter without duplicating the main filter, it does not have matching and tracking problems inherent in the master-and-slave tuning scheme. Furthermore, it consumes smaller silicon area if the LC passive filter is implemented monolithically on the chip. Simulations indicate the feasibility of this proposed tuning scheme for the gigahertz band filter operation and effectively correct for process variation.

4. REFERENCES

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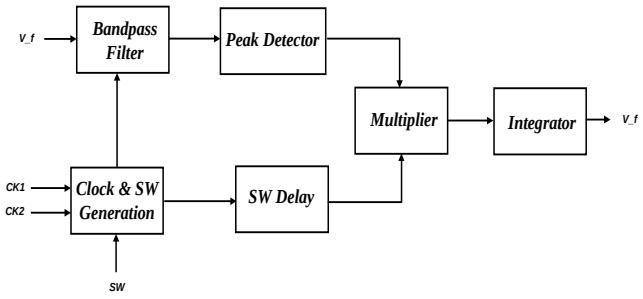

Figure 1. Frequency tuning block diagram

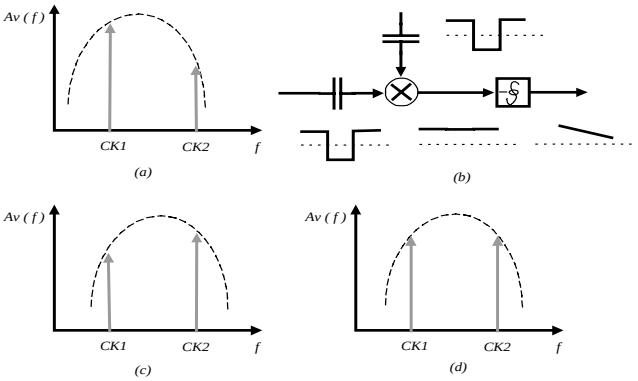

Figure 2. Synchronous rectification scheme

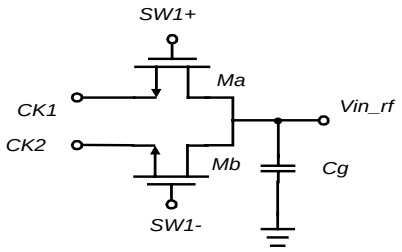

Figure 3. Input test signal selection

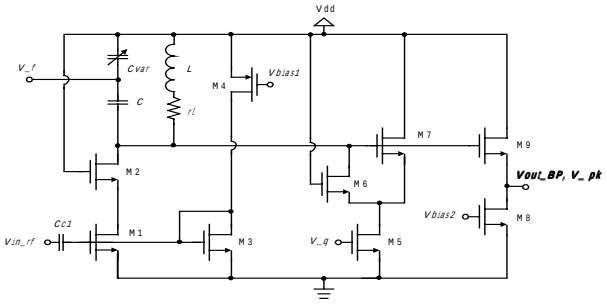

Figure 4. LC bandpass filter

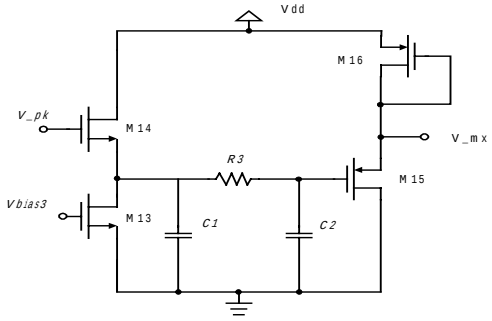

Figure 5. Peak amplitude detector

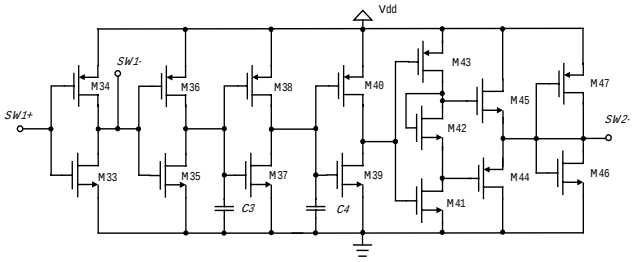

Figure 6. Clock generator and swing reduced clock driver

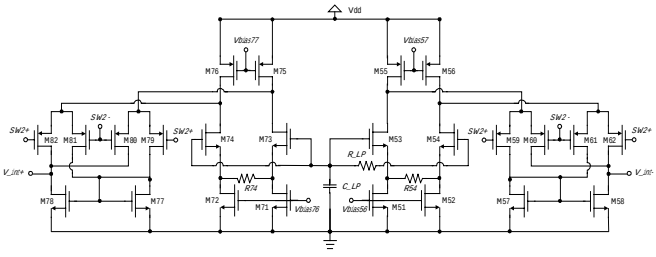

Figure 7. Gilbert cell multiplier

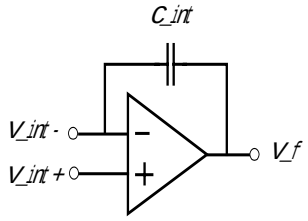

Figure 8. Op-amp Integrator

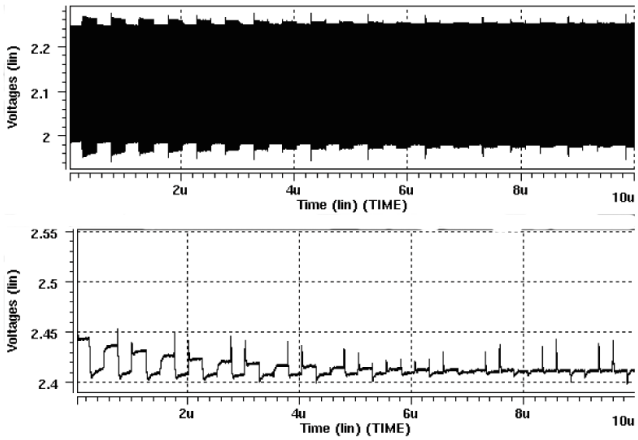

Figure 9. Outputs of bandpass filter and peak detector

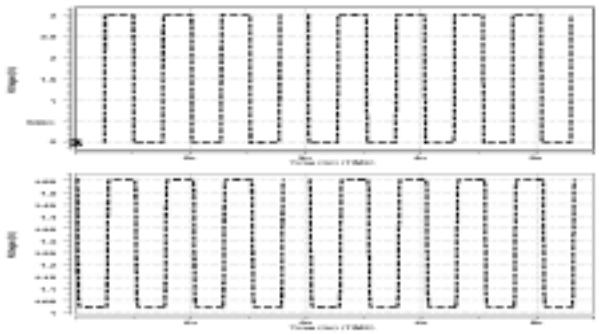

Figure 10. SW1+ and SW2+

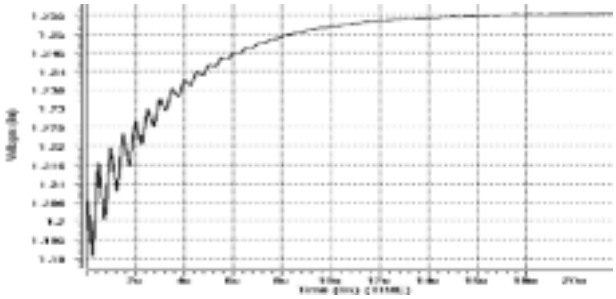

Figure 11. Tuning voltage to the varactor