

A CMOS Monolithic Image-Reject Filter

YUYU CHANG,¹ JOHN CHOMA, JR.¹ AND JACK WILLS²

¹Department of Electrical Engineering. University of Southern California, Los Angeles. CA 90089

²Information Sciences Institute. University of Southern California, Marina del Rey, CA 90292

E-mail: yuyuchan@usc.edu; johnc@usc.edu; jackw@isi.edu

Received June 27, 2000; Revised August 15, 2000; Accepted December 1, 2000

Abstract. A CMOS inductorless image-reject filter based on active RLC circuitry is discussed and designed-with the emphasis on low-noise, low-power, and gigahertz-range circuits. Two Q-enhancement techniques are utilized to circumvent the low Q characteristics inherent in the simple feedback circuit. The frequency tuning is almost independent of Q tuning, facilitating the design of the automatic tuning circuitry. The stability and the tuning scheme of the filter are also discussed. Simulations using $0.6~\mu m$ CMOS technology demonstrate the feasibility of the tunable image-reject filter for GSM wireless applications. Simulation results show 4.75 dB voltage gain, 9.5 dB noise figure, and -20~dBm~IIP3 at a passband centered at 947 MHz. The image signal suppression is 60 dB at 1089 MHz and the power consumption is 27 mW.

Key Words: RF filter, notch filter, CMOS continuous-time filter

1. Introduction

The rapid growth of the wireless communication and the rising demand for compact, low-cost, and lowpower radio frequency (RF) integrated circuit make a single chip solution highly desirable. In RF applications, wireless receivers most often use a heterodyne architecture consisting of a bandpass filter, a low noise amplifier, an image reject filter, and a mixer. At the present time, few of these components are integrated with digital baseband circuitry in commercial wireless products. RF filters required for band selection and image rejection are currently dominated by off-chip components such as ceramic or surface acoustic wave (SAW) filters. These components require additional I/O pins and often need impedance matching networks to work properly. In addition, performance may be limited by parasitic elements associated with semiconductor packaging.

The image-reject filter originates from the phenomenon that the mixer downconverts the frequency bands (the image signal and desired RF signal) symmetrically located above and below the local oscillator frequency to the same intermediate frequency (IF) and it, therefore, corrupts the desired RF signal, mandating the image reject filter to suppress the image signal. In

contrast, there is no image problem in direct conversion receivers, but problems with DC offset and phase noise have prevented their widespread use.

The desired overall image rejection in most RF systems is typically 70-100 dB. In applications using a high IF frequency, considerable image attenuation may be provided by the front-end bandpass filter. However, to achieve such a high image attenuation, the imagereject filter is usually realized by bulky, external, and passive components. This usually requires that the LNA needs to drive 50 Ω input impedance of the filter and the mixer needs to exhibit 50Ω input impedance. In addition, the passive components generally exhibit gain loss, thereby leading to large noise contribution to the system. In the literature [1-4], monolithic image rejection has been demonstrated by employing image-reject mixers which essentially exploit Hartley or Weaver architectures [5,6], as depicted in Fig. 1. The critical problems with such topologies are that the image suppression is very sensitive to gain and phase mismatches between two receiver paths due to the process and temperature variation. In addition, there exists a secondary image issue for Weaver architecture if the second downconversion is to non-zero IF. Therefore, the image suppression is typically in the range of 30-40 dB. An alternate approach to achieve substantial image suppression

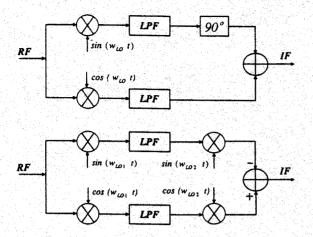


Fig. 1. Hartley and Weaver image-reject mixers.

is to exploit on-chip inductors [7]. The drawbacks of passive monolithic inductors are well known as large chip area and low inductor quality factor (Q) due to the resistive loss and capacitive coupling to the substrate [8].

In this paper, we propose a monolithic inductorless CMOS image-reject filter for RF image rejection to reach maximal integration level.

2. Filter Principle and Operation

2.1. Basic Passive Architecture

Consider a series LC resonator shown in Fig. 2, where C is a capacitor, L is an inductor, R_L is the parasitic resistance of the inductor, and Z_o is the loading impedance. The transfer function can be expressed as

$$\frac{V_o(s)}{I(s)} = Z_o \frac{s^2 + s(R_L/L) + 1/LC}{s^2 + s(R_L/L + Z_o/L) + 1/LC}$$
$$= Z_o \| R_L \quad \text{if } \omega = \omega_o = \sqrt{1/LC}$$

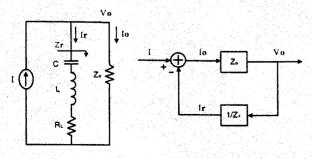


Fig. 2. A passive notch filter and feedback block diagram.

For a typical 10 nH on-chip inductor with O equal to 5 operating at 1 GHz, R_L is around 10 Ω . In order to achieve considerable gain attenuation at the resonant frequency, the loading impedance must be extremely small, which is a difficult design challenge at radio frequencies. Observe that this circuit configuration generates both complex zeros and poles at the same resonant frequency ω_o , but the notching effect of the zeros exceeds the limited gain caused by the poles, leading to gain attenuation. In VLSI design, there are other resistive and capacitive losses associated in the circuit, and these losses may cause the pole frequency to deviate from the zero frequency so that full pole/zero cancellation does not occur. Such filters exhibit possibly better notching effects at ω_o . This property will be clarified in later sections. We also note that if R_L and L are tunable, then the resonant frequency and gain attenuation can be controlled and tuned to correct for the VLSI process variation. In contrast, passive inductors usually are not tunable. To achieve the tunability, a lossless active inductor is presented in this work as a basic function block to realize a tunable notch filter, thus rejecting the RF image signal.

Alternatively, this circuit can be viewed as a feedback system [7]. The transfer function can be rewritten in another form as

$$\frac{V_o(s)}{I(s)} = \frac{Z_o}{1 + Z_o/Z_r}$$

and the corresponding feedback diagram is depicted on the right of the Fig. 2, where an error current I_o is generated from the difference of a current source I and a current I_r from the output voltage V_o . If $1/Z_r$ is of bandpass characteristic with a finite quality factor as

$$\frac{1}{Z_r} = G \frac{s(\omega_o/Q)}{s^2 + s(\omega_o/Q) + \omega_o^2}$$

where ω_o is the resonant frequency, Q is the quality factor of the filter, and G is the gain of the transfer function at ω_o . The overall closed-loop transfer function can be shown as

$$\frac{V_o(s)}{I(s)} = Z_o \frac{s^2 + s(\mathbf{b}_o/Q) + \omega_o^2}{s^2 + s(1 + GZ_o)(\omega_o/Q) + \omega_o^2}$$
$$= \frac{1}{1 + GZ_o} \quad \text{if } \omega = \omega_o$$

The above equation shows that if a bandpass filter is placed in the feedback loop, then the closed-loop configuration exhibits notch characteristic. It is worth noting that the numerator shows $1 + GZ_0$ reduction

in quality factor, leading to better stability. Substantial notching effect can be achieved if both the gain G and the loading impedance Z_o are increased, which is independent of the quality factor of the bandpass filter. The feedback elements are implemented by using series active LC resonator in this work.

2.2. Active Inductor with Loss Compensation

Fig. 3 illustrates an impedance load circuit used to realize a tunable active inductor. Z_{in} exhibits very low impedance at low frequencies due to the negative feedback formed by transistors M6, M7, and M8. When the operating frequency increases, the feedback is reduced and the impedance becomes inductive. Eventually, it decreases at higher frequencies due to the complex poles generated by the feedback circuits. Therefore, it demonstrates bandpass characteristics.

Assuming $g_m \gg g_{ds}$ for transistors and ignoring all non-dominant high-order terms, Z_{in} can approximately be expressed as

$$Z_{in}(s) \approx M \frac{s+D}{s^2 + sA + B} \tag{1}$$

where

where
$$A = g_{m8} \frac{N}{(g_{m8}c^2 + g_{m6}c_3c_4)^2}$$

$$B = \frac{g_{m6}g_{m7}}{c^2}$$

$$D = \frac{g_{ds}}{c_2 + c_3}$$

$$M = \frac{c_2 + c_3}{c^2}$$

$$N = g_{m7}g_{m8}c_2c^2 + g_{m6}g_{m8}c_3c^2 + g_{m6}^2c_3^2c_4$$

$$- g_{m6}g_{m7}c_4(c_1c_2 + c_1c_3) - g_{m6}c_5[g_{m8}c^2$$

$$+ g_{m6}c_3c_4 + g_{m7}c^2 + g_{m7}c_4(c_2 + c_3)]$$

$$c^2 = c_1c_2 + c_2c_3 + c_1c_3$$

$$c_1 = c_{gd5} + c_{db5} + c_{sb6} + c_{gs7} + c_{gb7}$$

$$c_2 = c_{gs6}$$

$$c_3 = c_{gb6} + c_{gd6} + c_{gd8} + c_{db8} + c_{db9} + c_{gd9}$$

$$c_4 = c_{db7} + c_{sb8} + c_{gs8}$$

$$c_5 = c_{gd7} + c_q$$

$$g_{ds} = \frac{g_{ds7}g_{ds8}}{g_{ms}} \left\| \frac{g_{ds9}g_{ds10}}{g_{m9}} \right\|$$

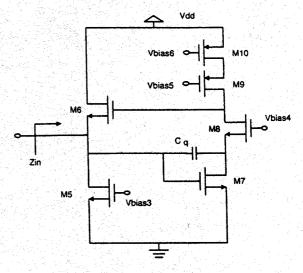


Fig. 3. The input impedance load with bandpass characteristics.

 c_1 , c_2 , c_3 , and c_4 represent accumulated parasitic capacitances in the circuit. c_5 represents an extra physical Q-enhancement poly-silicon capacitor c_q in shunt with the parasitic capacitance between the gate and the drain of the transistor M7. g_{ds} is the conductance at the gate of transistor M6 and is very small due to the feedback mechanism.

Accordingly, the center frequency of the bandpass impedance load is given by

$$\omega_p = \sqrt{\frac{g_{m6}g_{m7}}{c^2}} \tag{2}$$

and the quality factor is therefore equal to

$$Q_p = \frac{\sqrt{g_{m6}g_{m7}}}{cA} \tag{3}$$

Equation (2) shows that the center frequency ω_p of the filter transfer function is determined by the transconductance of the transistors M6, M7, and the parasitic capacitive effect exhibiting in the circuit. Here the transconductance of the transistor M6 is chosen as a prime candidate to be tuned by varying V_{bias3} while the other bias voltage sources remain constant. An observation that can also be made from equations (1) and (3) is that the Q_p can be boosted by increasing capacitor c_q in c_5 , thus decreasing N, decreasing A, finally increasing the quality factor. This approach is very effective in the sense that small c_q variation can cause large Q_p variation and furthermore the Q_p can be independently tuned without altering the center frequency

 ω_p in equation (2). Therefore, this tuning approach by inserting c_q can be viewed as the coarse Q_p tuning. Another Q-enhancement technique is to vary gm_8 by tuning V_{bias4} . Simulations show that the tuning of V_{bias4} has a similar effect as c_5 , but is not shown from the above equations due to the analytical complexity. This approach is used to tune the Q_p after c_q is added and can be viewed as a fine Q_p tuning.

Further insight can be gained by considering other high frequency parasitic poles and zeros implicitly presented in the circuit. Assuming the feedback loop is broken, increasing the values of the capacitor c_q and V_{bias4} generates more phase shift at the output unitygain frequency since the parasitic poles and/or zeros tend to move to lower frequencies, thereby decreasing the phase margin of the open-loop circuit and boosting the quality factor of the closed-loop circuit [9].

Both Q-enhancement approaches are combined to reach better tuning performance. Therefore, the tuning of the center frequency is provided by varying g_{m6} , and the Q_p tuning is obtained by physically inserting an extra capacitor c_q and electrically varying V_{bias4} .

In general, the center frequency formed by complex poles in the bandpass impedance load transfer function in equation (2) corresponds to the center frequency formed by complex zeros in the series *LC* filter

with only some frequency shift. The explanation will be provided in the next section.

2.3. Active Filter Architecture

The proposed notch filter for RF image rejection is depicted in Fig. 4. The input stage consists of a common-source cascode amplifier with a source degeneration resistor R_e to enhance the linearity of the notch filter. 50 Ω is chosen as a trade-off between linearity and direct noise contribution to the input-referred signal-to-noise ratio. The input stage is biased such that it not only offers voltage gain but also reduces the noise contributions of the following stages. In contrast, discrete notch filters usually exhibit gain loss. The capacitor c_n provides the notching function due to series resonance with the bandpass input impedance stage illustrated in Fig. 3.

To facilitate the derivation of the transfer function, a simplified circuit model is used in Fig. 5 to represent the input impedance at the drain of the transistor M2. Conceptually, a capacitor c_n is in series with the inductive element Z_{in} to generate a notching effect. c_p is the accumulated parasitic capacitance to the ground and R is the DC impedance level at the drain of transistor M2, respectively.

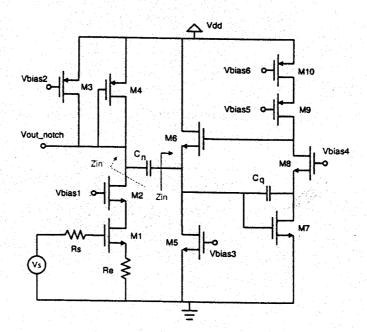


Fig. 4. The proposed notch filter.

-

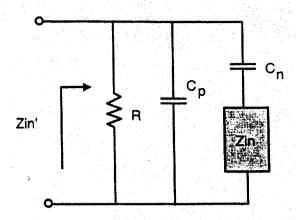


Fig. 5. A simplified model for the derivation of the notch filter transfer function.

Considering the output voltage established by the current flowing through Z_{in} , it can be shown that the transfer function of the notch filter is expressed as

ing capacitor c_n . Similar to the tuning of the bandpass impedance load, the tuning of ω_z is accomplished by varying V_{bias3} to tune g_{m6} . Equation (6) shows that the O tuning is achieved by adding c_a and varying V_{bias4} . The denominator of the equation (4) also reveals that there is a pair of complex poles which are located close to complex zeros as expressed in equation (5). Simulations show the quality factor of the poles increases with the quality factor of the zero. Therefore, the notching effect is somewhat attenuated by the complex poles and thus the notching depth is reduced. Simulations also show that increasing c_n can push the complex poles to higher frequency and decrease Q_p , but this further reduces ω . Iterative simulations must be performed to obtain an optimized c_n . In this work, we select $c_n = 0.15$ pF. Fig. 6 shows the wide ω_z tuning range this filter can achieve from 595 MHz to 1354 MHz with c_q equal to 0.35 pF, 0.2 pF, and 0.1 pF, respectively.

$$A_{v_{notch}}(s) = \frac{V_{out_notch}(s)}{v_s(s)} = \frac{g_{m1}}{1 + g_{m1}R_e} \cdot \frac{1 + c_n M}{c_n + c_p(1 + c_n M)}$$

$$\cdot \frac{s^2 + s\left(\frac{A + c_n DM}{1 + c_n M}\right) + \frac{B}{1 + c_n M}}{s^3 + s^2 \left\{\frac{1 + c_n M + (c_n + c_p)AR + c_n c_p DMR}{R[c_n + c_p(1 + c_n M)]}\right\} + s\left\{\frac{A + c_n DM + (c_n + c_p)BR}{R[c_n + c_p(1 + c_n M)]}\right\} + \frac{B}{R[c_n + c_p(1 + c_n M)]}$$
(4)

where

$$c_p = c_{gd2} + c_{db2} + c_{gd3} + c_{db3} + c_{db4}$$

$$R \approx 1/g_{m4}$$

The center frequency of the image-reject filter can be obtained from equation (1) and given by

$$\omega_z = \sqrt{\frac{g_{m6}g_{m7}}{c^2 + c_n(c_2 + c_3)}} \tag{5}$$

and the quality factor of the image-reject filter is therefore equal to

$$Q_z = \frac{\sqrt{[c^2 + c_n(c_2 + c_3)]g_{m6}g_{m7}}}{c^2 A + c_n g_{ds}}$$
 (6)

Comparing equations (5), (6), and equations (2), (3), it is obvious that both bandpass impedance load and notch filter share similar expressions for the center frequency and quality factor, except for the additional terms. Comparison also shows that the center frequency of the notch filter is smaller than that of the bandpass impedance load due to the insertion of a notch-

We have designed an image-reject filter for Global System for Mobile Communication (GSM) standard with a passband centered at 947 MHz. The first IF is set to 71 MHz with a high side injection local oscillator, leading to an image at 1089 MHz that must be suppressed. The IF equal to 71 MHz is selected so that the performance of this image-reject filter can be compared with regular off-the-shelf passive image-reject filters. Fig. 7 shows that the notching depth ranges from 15 dB to over 60 dB with V_{bias4} tuning from 2.5 V to 2.19 V while ω_z deviates from 1097 MHz to 1089 MHz. The frequency deviation is 8 MHz, corresponding to only 0.7% frequency shift. Therefore, the tuning sensitivity is 0.0056 V/dB. It is worth noting that the tunings of ω_r and Q_r are almost independent of each other. This independent relationship makes the design of the automatic tuning circuit much easier and feasible.

The voltage gain and noise figure (NF) in the desired signal band are equal to 4.75 dB and 9.5 dB, respectively. The linearity of the desired signal band can be determined by performing a two-tone test such

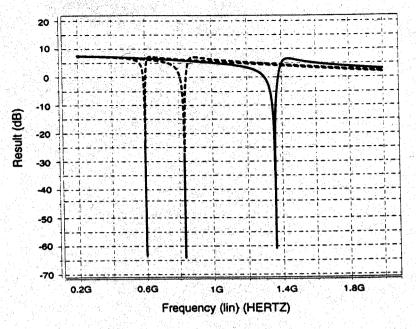


Fig. 6. The high-Q image-reject filter with center frequencies between 595 MHz and 1354 MHz.

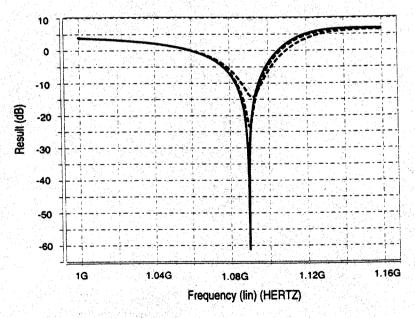


Fig. 7. The Q tuning with a ω_z at 1089 MHz.

that the third-order intermodulation products fall into the passband centered at 947 MHz where the frequency response of the filter shows little attenuation. We applied two small sinusoids at 945 MHz and 950 MHz, and input third-order intercept point (IIP3) is equal to $-20\,\mathrm{dBm}$. The linearity is a little bit small mainly due to

the non-linear amplifier stage formed by the transistors M5 to M10. The IIP3 can be increased by increasing g_{m6} and applying another source degeneration resistor to the transistor M7, but NF will be increased. Therefore, there is a linearity-noise trade-off. The power consumption is equal to 27 mW mainly contributed

Table 1. The performance metrics of the image-reject filter for GSM wireless standard.

Parameter	Simulation Result
Capacitor c _n	0.15 pF
Capacitor c_q	0.15 pF
Center frequency ω_z	1089 MHz
Gain at 947 MHz	4.75 dB
Noise figure	9.5 dB
IIP3	-20 dBm
Notch depth	60 dB
Notching tuning range	15-60 dB
$\Delta\omega_{z}$	0.7%
Power consumption	27 mW

by the input stage due to the noise consideration. The simulation results are listed in Table 1.

3. Filter Stability and Tuning Issues

The stability of the image-reject filter is analyzed using Routh-Hurwitz criterion. Directly applying Routh-Hurwitz criterion to the analysis of the pole locations in equation (1) is complicated and tedious. Instead, we approach this problem indirectly; we assume that we have tuned the Q_z of the filter to infinity, and we then evaluate the stability criterion based on:

For a third-order system to be stable,

$$q(s) = a_3 s^3 + a_2 s^2 + a_1 s + a_0$$

It is necessary and sufficient that

$$a_2a_1 > a_0a_3$$

It can be shown that if the complex zeros of the filter are located on the left half of the s-plane, then the filter is guaranteed to be stable if and only if

$$\frac{\overline{c_2 + c_3}}{g_{ds}} > R(c_n + c_p) \tag{7}$$

In our design, since g_{ds} is mainly determined by the output conductance of the PMOS cascode stage formed by M9 and M10, it is much smaller than R. Simulations also show that the capacitances on both sides of equation (7) are of the same order. Consequently, the above equation is automatically satisfied in this filter design. Accordingly, if the complex zeros are negative, the stability of the filter is guaranteed.

Additional tuning circuitry is required to be added to this proposed filter due to manufacturing variations. In addition, temperature fluctuations further aggravate the

situation. The master-slave tuning scheme is a common approach along with the OTA-C filters [10]. Unfortunately, this tuning scheme is unlikely to be suitable for giga-hertz band filters due to the strong dependence of the parasitic capacitances, leading to severe matching problems. An alternative approach, called adaptive filter tuning scheme [11] commonly used in digital signal processing applications, usually involves much more complicated computations and circuitry, and therefore increases the complexities of the filter. If transceivers use burst-mode transmission, filter can be tuned during the bursts by employing the self-tuned scheme [12]. This switching technique eliminates matching problems in the master-slave tuning scheme, thereby making it a better candidate for hight-frequency filter tuning.

4. Conclusion

The implementation of the RF monolithic image-reject filter is one of the main obstacles to achieve the singlechip solution. In this paper, a new fully-integrated tunable CMOS notch filter for RF image rejection has been analyzed, designed, and simulated using 0.6 μ m CMOS technology. The simulated design is targeted at GSM wireless standard. This simple architecture allows an image-reject filter with ω_z reaching gigahertz frequency range and a high quality factor to be feasible by considering the distributed high frequency parasitic capacitances and characteristics of transistors as filter elements. Two Q-enhancement techniques are adapted to achieve wide Q tuning range. This proposed filter does not have matching problems associated with image-reject mixers, and so it can achieve higher image rejection. However, precise frequency and Q tunings become critical. Therefore, automatic tuning circuitry is needed to compensate for the process variation and temperature fluctuation.

References

- McDonald, M. D., "A 2.5 GHz BiCMOS image-reject front end." ISSCC Dig. Tech. Papers, pp. 144-145, February 1993.
- Baumberger. W., "A single-chip image rejecting receiver for the 2.44 GHz band using commercial Ga-MESFET technology." IEEE J. Solid-State Circuits 29, pp. 1244–1249, October 1994.
- Pache, D., Fournier, J. M., Billiot, G. and Senn, P., "An improved 3 V 2 GHz BICMOS image reject mixer IC." IEEE J. Custom Integrated Circuit Conf., Section 6.3. pp. 95–98, 1995.

- Pandula, L., "Image reject and image canceling mixers." RF Design Mag., pp. 60-65, April 1995.
- 5. Hartley, R., "Modulation System." U.S. Patent 1,666,206, April 1928.
- Weaver, D. K., "The third method of generation and detection of single-sideband signals," in *Proc. IRE* 44, pp. 1703–1705, December 1956.
- Macedo, J. and Copeland, M., "A 1.9-GHz silicon receiver with monolithic image filtering." *IEEE J. Solid-State Circuits* 33(3), pp. 378–386, March 1998.
- 8. Long, J. and Copeland, M., "The modeling, characterization, and design of monolithic inductor for silicon RF IC's." *IEEE J. Solid-State Circuits* 32(3), pp. 357–369, March 1997.
- Choma, J. Jr., Electrical Network: Theory and Analysis. John Wiley and Sons, Inc., New York, 1985.
- Tsividis, Y. and Voorman, J., Integrated Continuous-Time Filters. IEEE Press, New York, 1993.
- 11. Shoval, A., Snelgrove, W. and Johns, D., "A 100-Mb/s BiCMOS adaptive pulse-shaping filter." IEEE J. Selective Areas in Communications: Special Issue on Copper Wire Access Technologies for High-Performance Networks, 1995.
- 12. Tsividis, Y., "Self-tuned filter." Electronics Letters 17(12), pp. 406-407, June 1981.



Yuyu Chang was born in Miaoli, Taiwan in 1969. He received his B.S. degree from the Department of Electronics Engineering, Chung Yuan Christian University, Taiwan, in 1992 and M.S. degree from the Department of Electrical Engineering, University of Southern California, Los Angeles, in 1996, where he is currently pursuing the Ph.D. degree.

Since 1996 he has been with USC/Information Sciences Institute, Marina de Rey, California, where he is a Research Assistant and is involved in both analog front-end design for communication applications and

digital microprocessor-in-memory design. He received the Best Paper Award from the Southwest Symposium on Mixed-Signal Design in 2000. His research interest includes CMOS RF filter and transceiver design.



John Choma, Jr. earned his B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Pittsburgh in 1963, 1965 and 1969, respectively. He is currently a professor of Electrical Engineering-Electrophysics at the University of Southern California. He authors or coauthors some 120 journal and conference papers and is the 1994 recipient of the Prize Paper Award from the IEEE Microwave Theory and Techniques Society. He is also the recipient of the 1999 IEEE Circuits And Systems Society Education Award. He is the author of a Wiley Interscience text on electrical network theory. He has contributed several chapters to four edited electronic circuit texts, and he was an area editor of the IEEE/CRC Press Handbook of Circuits and Filters. He has served the IEEE Circuits And Systems Society as a member of its Board of Governors, its vice president for Administration, and its president. He has also been an associate editor and editor in chief of the IEEE Transactions On Circuits And Systems, Part II and a former regional editor of the Journal of Circuits, Systems, and Computers. He is an associate editor of the Journal of Analog Integrated Circuits and Signal Processing.

His research interests include wideband analog and high speed digital integrated circuit design, behavioral analysis of electronic systems, integrated device modeling, and engineering education in the circuits and systems areas. A Fellow of the IEEE, he is the recipient of numerous teaching awards, and he is a "Distinguished Lecturer" in the IEEE Circuits And Systems Society.



Jack Wills was born in Long Beach, California in 1951. He received his B.A. in Mathematics from UCLA

in 1972. He received his M.S.E.E. from UCLA in 1985 and his Ph.D. in electrical engineering from UCLA in 1990.

He has worked at the University of Southern California Information Sciences Institute since 1995 where he is a senior researcher. Dr. Wills is a member of the IEEE, the Audio Engineering Society, and Phi Beta Kappa.

He is presently working on low power TDMA communications as part of the SensIT program as well as high speed chip to chip interconnect for the Data-IntensiVe Architecture (DIVA) project.